

N77-32352

SOLID STATE Ku-BAND SPACECRAFT TRANSMITTERS

W. R. Wisseman
H. Q. Tserng
D. J. Coleman
F. H. Doerbeck

Texas Instruments Incorporated
Central Research Laboratories
P. O. Box 5936
Dallas, Texas 75222

5-26-77
Figure 29, p. 68
used in 1376 Interim
as Figure 1.

March 1977

Final Report for Period December 1974 - February 1977

REPRODUCIBLE COPY
(FACILITY CASSETTE COPY)

Prepared for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.	
4. Title and Subtitle Solid State Ku-Band Spacecraft Transmitters		5. Report Date March 1977	
		6. Performing Organization Code	
7. Author(s) W. R. Wisseman, H. Q. Tserng, D. J. Coleman, F. H. Doerbeck		8. Performing Organization Report No. 08-77-11	
9. Performing Organization Name and Address Texas Instruments Incorporated Central Research Laboratories P. O. Box 5936 Dallas, Texas 75222		10. Work Unit No.	
		11. Contract or Grant No. NAS5-20894	
12. Sponsoring Agency Name and Address Goddard Space Flight Center Greenbelt, Maryland 20771 Dom Santarpia, Code 715		13. Type of Report and Period Covered Final Report for Period December 1974 - February 1977	
		14. Sponsoring Agency Code	
15. Supplementary Notes			
16. Abstract <p>The objective of this program was to develop a Ku-band solid state transmitter. The transmitter was to consist of GaAs IMPATT and Read diodes operating in a microstrip circuit environment to provide amplification with a minimum of 63 dB small-signal gain and a minimum compressed gain at 5 W output of 57 dB.</p> <p>The work discussed in this report includes Schottky-Read diode design and fabrication, microstrip circuit and circulator optimization, preamplifier development, power amplifier development, dc-to-dc converter design, and integration of the breadboard transmitter modules.</p> <p>A four-stage power amplifier in cascade with a three-stage preamplifier had an overall gain of 56.5 dB at 13.5 GHz with a power output of 4.5 W. A single-stage Read amplifier delivered 5.9 W with 4 dB gain at 22% efficiency.</p> <p>The microwave performances of each of the breadboard transmitter modules delivered at the end of Phases I and II are also presented, along with problem identification and recommendations for future work.</p>			
17. Key Words Transmitter, Solid State, Ku-Band, IMPATT Diodes, Schottky-Read Diodes, Microwave Integrated Circuits, Microstrip Circulators		18. Distribution Statement	
19. Security Classif. (of this report) UNCLASSIFIED	20. Security Classif. (of this page) UNCLASSIFIED	21. No. of Pages 95	22. Price

TABLE OF CONTENTS

<u>SECTION</u>	<u>PAGE</u>
I INTRODUCTION AND SUMMARY	1
II READ DIODE FABRICATION	5
A. Device Physics	5
B. Gallium Arsenide Materials Growth	9
C. Device Fabrication and Evaluation	14
1. Slice Optimization	14
2. Fabrication Procedure	22
3. Evaluation	30
a. Voltage Mapping	31
b. Oscillator Performance	32
c. IMPATT Fabrication and Testing	37
d. Doping Profiles	38
D. Reliability Considerations	40
A. Introduction	45
B. Phase I Accomplishments	45
1. MIC Circulator	46
2. Preamplifier Design and Performance	50
3. Power Amplifier Design and Performance	58
4. Dc Power Supply Design	71
5. Breadboard Transmitter Module	74
C. Critical Design Problems	84
D. Phase II Breadboard Transmitter Module Development	85
IV CONCLUSIONS	92
REFERENCES	95

LIST OF ILLUSTRATIONS
(Continued)

<u>FIGURE</u>		<u>PAGE</u>
1(a)	Schottky-Read Diode	6
1(b)	Doping Profile	6
1(c)	Electric Field Distribution	6
2	Epitaxial Growth System with Sliding Substrate Reactor	10
3	Sliding Substrate, Abrupt Junction Epitaxial Reactor	11
4	Doping Profile of Low-High-Low Read Diode Structure	15
5(a)	GaAs Slice in Early Stage of Anodic Oxidation Thinning	18
5(b)	Electric Field Distribution Through Center of Slice	18
6(a)	GaAs Slice Near Completion of Anodic Oxidation Thinning	19
6(b)	Electric Field Distribution Through Center of Slice	19
7	Anodic Oxidation Setup	21
8	Plated Heat Sink Fabrication Procedure	24
9	Metallurgical Section of a Plated Heat Sink Diode Soldered to Cu Block	26
10	Optical Photograph of a Read Diode Mesa Coated with Liquid Crystal, Showing the Nonsymmetric Isotherm Indicative of Nonuniform High-Layer Thickness	29
11(a)	Diode Waveguide Cavity	33
11(b)	Bias Circuit	33
12	Output Power and Efficiency of a Ku-Band Read Diode Operating at 13.6 GHz	35
13	Doping Profiles of Ku-Band Read Slices	36
14	Doping Profiles of Ku-Band Read Slices	41
15	Doping Profiles of Ku-Band Read Slices	42
15	Photograph of a Test Fixture for a Microstrip Circulator	48
17	Characteristics of an X/Ku Band MIC Circulator	49
18	Photograph of the Advanced Integrated Preamplifier	52
19	Performance Characteristics of the Preamplifier Shown in Figure 18	53
20	Third-Order Intermodulation Product vs Input Level at Lower Band Edge of the Preamplifier	55

LIST OF ILLUSTRATIONS
(Continued)

<u>FIGURE</u>		<u>PAGE</u>
21	Third-Order Intermodulation Product vs Input Level at Band Center of the Preamplifier	56
22	Temperature Performance of the Preamplifier	57
23	Gain-Frequency Response of a Single-Stage Schottky-Read Microstrip Amplifier	60
24	Rf Performance of a Single-Stage Schottky-Read Amplifier	61
25	Bias Characteristics of a Single-Stage Schottky-Read Amplifier	62
26	Rf Performance of a Double-Mesa, Single-Stage Schottky-Read Amplifier	64
27	Gain Compression Characteristics of a Double-Mesa Schottky-Read Amplifier at Two Frequencies	65
28	Operating I-V Characteristics of a Schottky-Read Amplifier . . .	66
29	Photograph of a Four-Stage Power Amplifier	68
30	Gain-Frequency Response of a Four-Stage Power Amplifier	69
31	Gain-Frequency Response of the Second Four-Stage Power Amplifier	70
32	Schematic Diagram of the dc-to-dc Converter	72
33	Schematic Diagram of the Voltage Regulator	73
34	Bias Networks for the Cascaded Amplifier	75
35	Block Diagram of Transmitter Configuration	76
36	Microwave Performance of the Cascaded Amplifier I	77
37	Microwave Performance of the Cascaded Amplifier II	78
38	Photograph of the Breadboard Transmitter Module Showing the Individual Components	80
39	Photograph of the Complete Breadboard Transmitter Module	81
40	Gain Compression Characteristics of the Breadboard Module . . .	83
41	Schematic Diagram of a Stabilization Circuit for Read Amplifier Operation	87

LIST OF ILLUSTRATIONS
(Continued)

<u>FIGURE</u>		<u>PAGE</u>
42	Schematic Diagram of a Power Supply Squelch Circuit	88
43	Photograph of the Phase II Breadboard Module	90
44	Gain-Frequency Response of Phase II Breadboard Transmitter	91

LIST OF TABLES

<u>TABLE</u>		<u>PAGE</u>
I	Transmitter Design Goals	2
II	Performance Comparison of Single 150 μ m (Nominal) Diameter Diodes from Various Wafers	43

SECTION I

INTRODUCTION AND SUMMARY

The work presented in this report was performed under Contract No. NAS5-20894 to develop a solid state Ku-band spacecraft transmitter. The performance design goals for the transmitter are summarized in Table I. Development of a multistage reflection-type amplifier was selected as the approach to be followed for achieving the goals. It was determined that GaAs IMPATT and Schottky-Read diodes were the only solid state microwave devices available with performance characteristics compatible with the program requirements of 5 W power output at an overall transmitter efficiency of 10%. A microwave integrated circuit implementation of the circulator and impedance matching network functions was established as the means of realizing the small transmitter volume.

The first phase of the program, which ended with the delivery of a bread-board model nine months after contract award, included: Schottky-Read diode design and fabrication, microstrip circuit and circulator optimization, pre-amplifier development, power amplifier development, and a dc-to-dc converter design. The Schottky-Read diode design task included the effort involved in the epitaxial growth of the Read profile in GaAs and the fabrication technology associated with multiple-mesa plated heat sink diodes. The rf transmitter design task included work in three functional areas. The first was concerned with the design of broad bandwidth MIC circulators at Ku-band for use with IMPATT and Schottky-Read diodes to form reflection-type amplifier stages. The second was associated with the integration of three amplifier stages to create a preamplifier producing 36 dB of gain at input signal levels of -20 dBm or less. The third area represented a significant design challenge in the requirement to operate high power, high efficiency Schottky-Read diodes in a power

TABLE I

Transmitter Design Goals

<u>Parameter</u>	<u>Specification</u>
Center frequency	13.525 GHz
Bandpass (1 dB)	13.400 to 13.650 GHz
Bandpass ripple	±0.4 dB maximum
Gain	
(threshold to -30 dBm)	63 dB minimum
(-20 dBm)	57 dB minimum
(rate of change)	≤ 0.2 dB/10 MHz
Intermodulation products (for two -33 dBm cw signals separated by 10 MHz)	≤ 14 dBm at full gain
Maximum power available	50 W at 28 ± 1 V dc (negative terminal ground)
Operating temperature range	0 to 50°C
Spurious radiation	< -20 dBm
Cooling	Conducting heatsink only
Total volume	1000 cm ³ maximum
Connectors	Waveguide or OSM
General	Rugged, lightweight, capable of long- term unattended operation (space qualification not required)

amplifier configuration with 21 dB of gain at an output power of 5 W. The spacecraft transmitter also included a dc-to-dc converter to step up the nominal 28 volt dc supply to the value of 55 volts required for IMPATT and Schottky-Read diode operation. The design of the converter was an integral part of the first phase of the program.

A major part of the program was devoted to the task of GaAs materials growth and Read diode design and fabrication. Several slices produced devices that meet the performance criterion of greater than 2 W output power of 20% or greater efficiency. Material from one or two of these slices was also processed in a multiple mesa configuration to provide the 4 W device capability required for the final stage of the power amplifier. A Ku-band MIC circulator was designed and successfully incorporated in a three-stage reflection-type amplifier. The amplifier meets the performance specifications for the transmitter preamplifier (36 dB gain with a 1 dB bandwidth of 400 MHz). A single-stage Schottky-Read amplifier capable of 2 W cw output power with 6 dB gain and 22.4% power-added efficiency has been demonstrated at the frequency band of the transmitter. A single-stage, double-mesa Read amplifier was built that delivered 5.9 W with 4 dB gain at 22% efficiency at 13.5 GHz. A similar amplifier was used as the fourth stage (output) of a power amplifier that had 21 dB gain with an output power of 4.5 W. When this four-stage power amplifier was cascaded with a preamplifier, a total gain of 56.5 dB was obtained. A breadboard transmitter with an integral dc power supply that accepts 28 ± 1 V was delivered at the end of Phase I. The output power of this transmitter was 3 W with 55 dB gain over the required frequency band. The input power level was 45 W, and the module volume was 991 cm³.

At the end of Phase I, a contract modification was proposed and approved to redirect the program effort toward finding solutions to certain technical problems uncovered during Phase I of the program. At the end of the contract, an improved breadboard transmitter module was delivered in place of the two spacecraft transmitters originally scheduled.

The Phase II breadboard transmitter module delivered at the end of the contract is capable of providing a small signal gain in excess of 60 dB and a compressed gain of 48 dB at an output power of 2 W across the 13.4 to 13.65 GHz frequency band. Due to the lack of suitable high-power, high-efficiency diodes near the end of Phase II, the 5 W output power goal was not reached for the Phase II model. However, some design improvements were made with regard to the other aspects of the transmitter operation. The most notable improvement of the Phase II model was the incorporation of a power supply squelch circuit to ensure unconditionally stable operation of the transmitter.

The remainder of this report is organized as follows. Device design and materials growth are discussed in Section II. The overall design considerations for the spacecraft transmitter are covered in Section III. Section IV summarizes conclusions drawn from the results of the experimental and theoretical investigation carried out during this contract period and recommendations for future work.

SECTION II

READ DIODE FABRICATION

The fabrication of GaAs Read diodes for Ku-band operation has proved to be a major impediment to successful design and testing of the spacecraft transmitter. This unforeseen difficulty received extensive investigation throughout the program. Materials preparation and device fabrication techniques and procedures have been critically evaluated, and no item that would singularly limit performance has been identified. In this section, the device design principles, materials growth procedures, and device fabrication techniques are briefly reviewed. A discussion of the measurable device parameters as related to these designs and techniques is presented, the values are compared with standards, and potential causes of difficulty are identified.

A. Device Physics

The basic high-low GaAs Read diode structure is illustrated in Figure 1(a). It consists of a Schottky barrier contact to an appropriately doped n-type epitaxial active layer with an ohmic contact to the heavily doped substrate. An idealized doping profile for a high-low Read diode is shown in Figure 1(b). The IMPATT diode differs from the Read in that the doping of the active layer is uniform at a level n , where $n_2 < n < n_1$ for the same frequency of operation. When either type of diode is reverse-biased to a sufficiently high level, avalanche breakdown occurs in a layer adjacent to the Schottky barrier contact as shown in Figure 1(c) for the Read diode. This results in a charge pulse that traverses the relatively long drift region to the ohmic collecting contact. Read showed that under these conditions the diode exhibits negative resistance that is maximum at a frequency corresponding to half the inverse transit time.¹ A modified version of the expression derived by Read for a diode operating under these conditions is given by

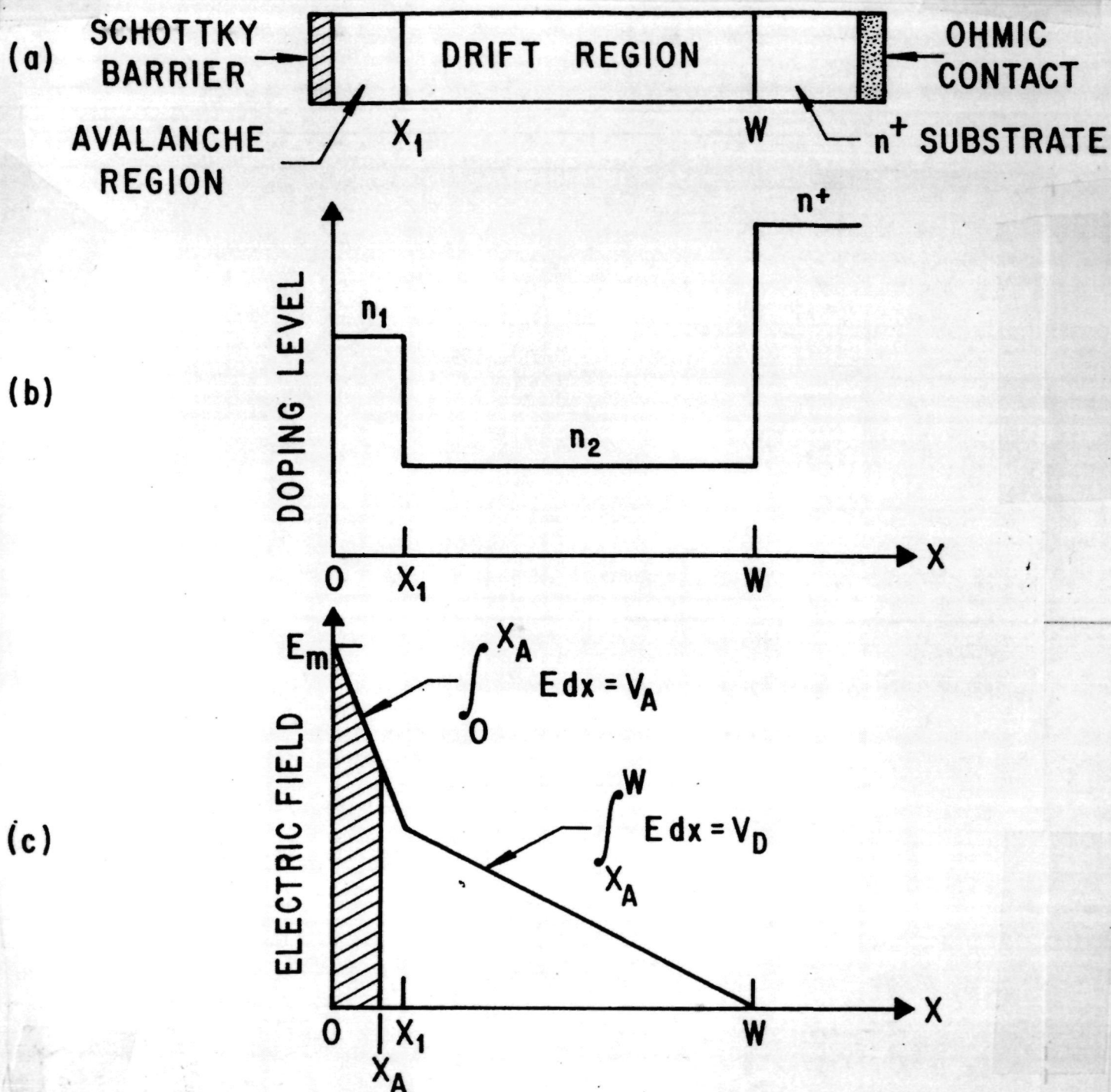


Figure 1 Schottky-Read Diode. (a) Diode Structure, (b) Doping Profile, (c) Electric Field Distribution.

$$\eta = \frac{V_D}{\pi(V_A + V_D)}, \quad (1)$$

where V_A is the voltage drop across the avalanche region and V_D is the voltage drop across the drift region. Maximum efficiency is achieved when V_A is small. The equation relating the drift length, W , to the operating frequency, f , is

$$W = \frac{34.4}{f} \mu\text{m} \quad (2)$$

for a 200°C operating temperature (f is in GHz), where the constant was obtained from experimental data.²

The maximum efficiency obtainable with an IMPATT diode is significantly lower than that for a Read diode because the uniformly doped IMPATT has a relatively wide avalanche region with a correspondingly high value for V_A . This results in a lower value for the theoretical efficiency calculated from Equation (1). The reduction in V_A achieved with the high-low structure can be realized with other doping profiles, most notably the low-high-low structure, which uses a thinner, more heavily doped high region buried beneath a lightly doped surface layer. In this structure the highly doped layer terminates the avalanche region and reduces the field strength in the drift layer to a value that falls to zero in a length appropriate to the desired frequency. Experimentally, efficiencies of 10 to 15% are obtained for uniform GaAs IMPATTs, while efficiencies in the 20 to 30% range are observed for both high-low and low-high-low GaAs Read diodes. This means that in order for the transmitter output power and maximum dc input power specifications to be met, Read diodes must be used in the final high-power amplifier stages. The diode requirements for the preamplifier stages are not critical and can be satisfied with either type of diode. A breakdown analysis procedure has been used to evaluate various Read diode doping profiles to determine the optimum structure for a particular frequency.

This approach, which involves applying the avalanche breakdown condition to specific doping profiles, has proved very useful for X-band diodes.² In the calculations, Equation (2) is used to determine the breakdown depletion depth for the desired operating frequency, with Equation (1) being used to calculate the efficiency.

For the Ku-band calculations, the transit length, W , was taken to be $3.0 \mu\text{m}$ by scaling up in frequency from the transit length required experimentally for x-band diodes. The calculations were then carried out for a series of different values for n_1 , n_2 , and x_1 (see Figure 1). A fairly wide range of n_1 , n_2 , x_1 combinations was calculated to give efficiencies over 20%. As a starting point for the initial materials specification, the values $n_1 = 10^{17} \text{ cm}^{-3}$, $n_2 = 5 \times 10^{15} \text{ cm}^{-3}$, and $x_1 = 0.4 \mu\text{m}$ were chosen. The calculations show that, for given values of n_1 and n_2 , the value of x_1 required for optimum microwave performance is extremely critical. The maximum allowable variation about the desired value is approximately $\pm 5\%$, with less variation being desirable. Since n_1 and n_2 may vary across an epitaxial slice and from run to run, x_1 cannot be precisely specified in advance of the materials growth. For this reason, the approach used at TI is to grow the high layer to a thickness greater than that required for the expected values of n_1 and n_2 , and then reduce this thickness by etching until the optimum thickness is reached.

It is necessary to consider the power handling capability of the diode as well as the efficiency in arriving at diode structures that will meet the transmitter requirements. In a subsection that follows, the plated heat sink procedure for diode fabrication is described. This technique incorporates a "flip-chip" geometry where the Schottky barrier is in direct contact with a high thermal conductivity heat sink metal. This results in rapid heat removal and maximum power-handling capability. The plated heat sink approach also makes it convenient to reduce the diode thermal resistance still further by combining several small mesas to give the same total device area and impedance as a large single-mesa device.

B. Gallium Arsenide Materials Growth

Growth of epitaxial GaAs structures for the Read diodes was accomplished with the vapor phase system shown in Figure 2. This system uses the $\text{GaAsCl}_3/\text{H}_2$ process, which is generally known to provide the low background impurity level that is essential for high mobility epitaxial layer. With a high AsCl_3 mole ratio, this process is capable of growing material with background concentration below 10^{13} cm^{-3} .

Read diodes require abrupt doping level transitions between the high and the low layers. These fast transitions were accomplished with a dual deposition zone reactor, shown schematically in Figure 3. The temperatures of the two deposition zones are maintained at the same value (760°C); hence, the layers are grown in both zones under conditions that are very similar with respect to gas composition and supersaturation. The only intentional difference between the two zones is the steady state dopant partial pressure. In the upstream deposition zone a sulfur partial pressure is established that is suitable for the growth of the drift layer of the Read structure, i.e., 1 to $10 \times 10^{15} \text{ cm}^{-3}$. In the downstream deposition region a higher dopant partial pressure is maintained by a separate dopant inlet. Layers grown in this region have doping levels appropriate for the avalanche region of the Read structure.

External magnetic coupling allows the substrates to be rapidly translated from one growth region to the other. Because this translation time is short (approximately two seconds), only a small amount of GaAs is deposited during the transition, and an abrupt doping level is achieved. This approach avoids gas dispersion and residence time problems associated with the more commonly used techniques of gas stream switching or dopant concentration manipulation with a single gas stream.

*half-tone.
excluded*

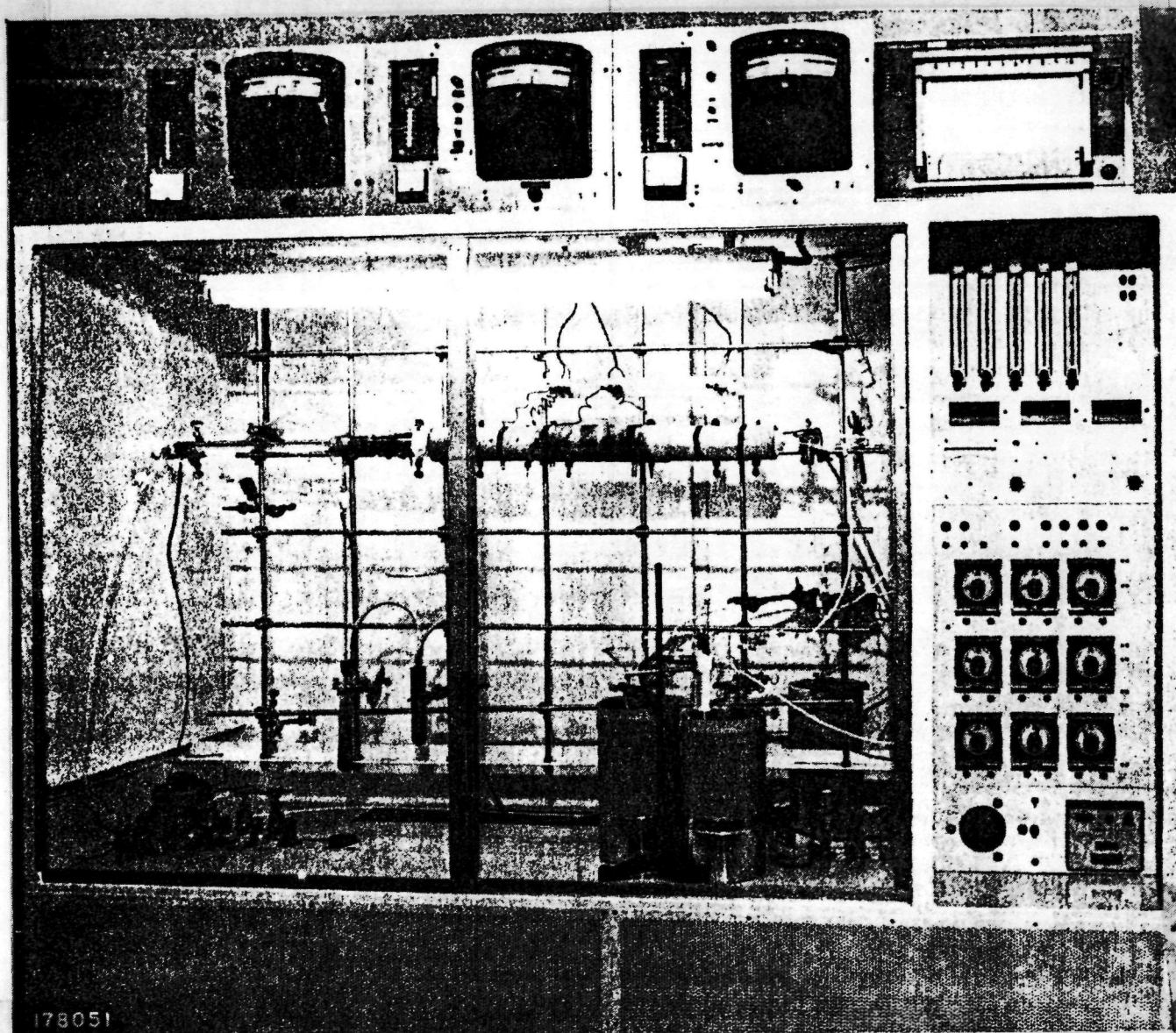


Figure 2 Epitaxial Growth System with Sliding Substrate Reactor

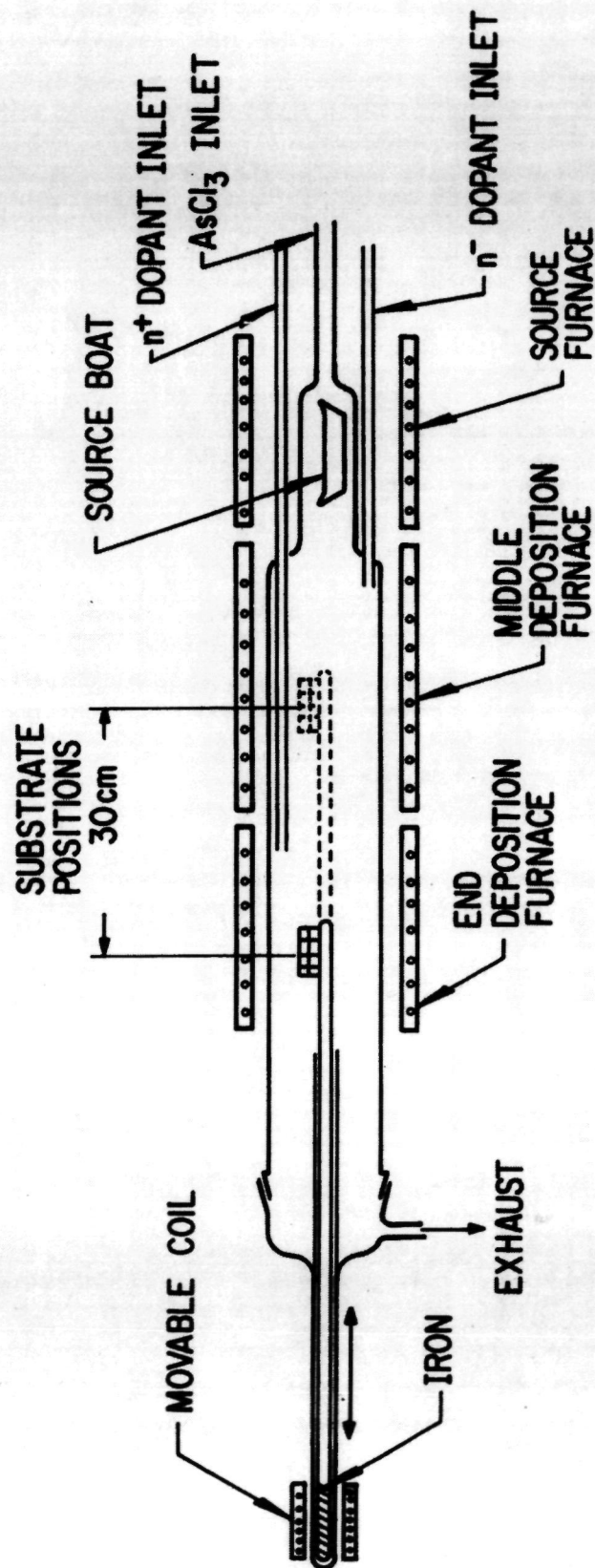


Figure 3 Sliding Substrate, Abrupt Junction Epitaxial Reactor

The Read structures grown for this program were the high-low type. An additional high layer is deposited first. This high layer serves as a buffer layer, separating the active part of the device from the relatively imperfect GaAs substrate. This buffer layer is grown in the downstream deposition zone and therefore has the same doping level as the high layer. Tellurium-doped GaAs substrate material for this program was purchased from commercial suppliers. The specifications called for polished slices, 0.38 mm (15 mils) thick, oriented 2° off {100} toward the nearest {110} plane; resistivity $< 1.5 \times 10^{-3}$ ohm-cm; and doping level $N = 1$ to 2×10^{18} cm⁻³. Immediately before the substrates were loaded into the reactor, they were etched in an aged solution of 8 parts H₂SO₄, 1 part H₂O, 1 part H₂O₂.

The epitaxial structures were evaluated by the following techniques. (1) A strip was cleaved from the GaAs slice and etched. The stained cross section was then inspected with a high-power microscope to determine the thickness of the deposited layers. (2) A step-etched sample was tested with a two-point probe. The breakdown voltage indicated the approximate doping levels. (3) Gold dots were plated on the step-etched sample, and the carrier concentration profile was obtained from a commercial profiler. Several profiles are discussed in detail in Section II.C (See Figures 13, 14, and 15).

The initial series of Ku-band structures was grown to the following specifications:

<u>Layer</u>	<u>Thickness (μm)</u>	<u>Doping Level (cm⁻³)</u>
High	0.8	1×10^{17}
Low	3.0	5×10^{15}
Buffer	4.0	1×10^{17}

The high layer was always grown to a thickness greater than specified and later etched to the desired thickness, as discussed in the following section.

In an effort to optimize device performance, a series of epitaxial runs was made, varying the doping of the drift region between 10^{15} cm^{-3} and 10^{16} cm^{-3} and that of the avalanche region between $5 \times 10^{16} \text{ cm}^{-3}$ and $2 \times 10^{17} \text{ cm}^{-3}$. It is known that the GaAs crystal perfection can be degraded if the tellurium concentration approaches $2 \times 10^{18} \text{ cm}^{-3}$. Higher etch pit densities caused by Te precipitates have been observed, and these defects can offset the quality of epitaxial structures. Therefore, experiments were performed with substrate slices having a doping level below 10^{18} cm^{-3} . The increased substrate resistivity leads to higher device resistance; furthermore, it requires replacement of the Schottky back contact with an alloyed contact. No conclusive evidence could be found for a correlation between substrate doping and device performance.

Throughout the program, attention was directed toward improving the reactor reliability, the epilayer surface quality, and the layer thickness uniformity. The $\text{AsCl}_3/\text{Ga}/\text{H}_2$ systems suffer from the fact that the arsenic-saturated gallium source is changing from run to run and that it requires regular additions of gallium with subsequent saturation. A reduction of the AsCl_3 bubble temperature to 0°C was found to have the following benefits:

- (1) The consumption of gallium source material was reduced, allowing more runs under similar source conditions.
- (2) The deposition of GaAs on the reactor quartz walls was reduced, leading to more stable growth rates.
- (3) The lower AsCl_3 consumption allowed more runs between refills of the AsCl_3 bubbler.

Similar results could have been obtained by the addition of hydrogen downstream from the AsCl_3 bubbler, but at the expense of additional gas lines, flow meters, etc.

Experiments with different substrate holders were performed to improve the epitaxial layer uniformity. Best results were obtained with an arrangement that places the GaAs substrate perpendicular to the gas flow direction. The thickness of the drift layer, measured microscopically along a cleaved stripe taken from the 2 cm long substrate, showed thickness variations of less than $\pm 7\%$, including the error of the microscopic readings.

As discussed in the section dealing with device evaluation, the microwave results obtained from high-low structures were inconsistent. For this reason, attention has recently been focused on the low-high-low structures. The epitaxial reactor was modified so that a gas volume of approximately 0.2 cm^3 , containing high concentration of sulfur, can be injected into the gas stream which controls the doping concentration in the upstream growth position. The doping profile of a recently grown sample is presented in Figure 4. Two layers were grown; the buffer layer (thickness $\sim 5 \mu\text{m}$, $N \sim 2 \times 10^{17} \text{ cm}^{-3}$) and the drift layer thickness $\sim 4.5 \mu\text{m}$, $N = 3 \times 10^{15} \text{ cm}^{-3}$). Toward the end of the drift layer growth, the doping pulse was injected. The profile shown in Figure 4 was composed from data obtained from a step-etched sample. The peak concentration is $7 \times 10^{17} \text{ cm}^{-3}$; the half-width is 200 \AA . These experiments proved that this modified reactor is capable of producing low-high-low Read structures.

C. Device Fabrication and Evaluation

1. Slice Optimization

Control of the thickness of the high layer to better than $\pm 5\%$ is critical to achieving optimum Read diode performance. Since the desired layer thickness is typically 4000 \AA , the maximum allowable variation is $\pm 200 \text{ \AA}$. For the best performance, variations should probably be kept within 100 \AA .

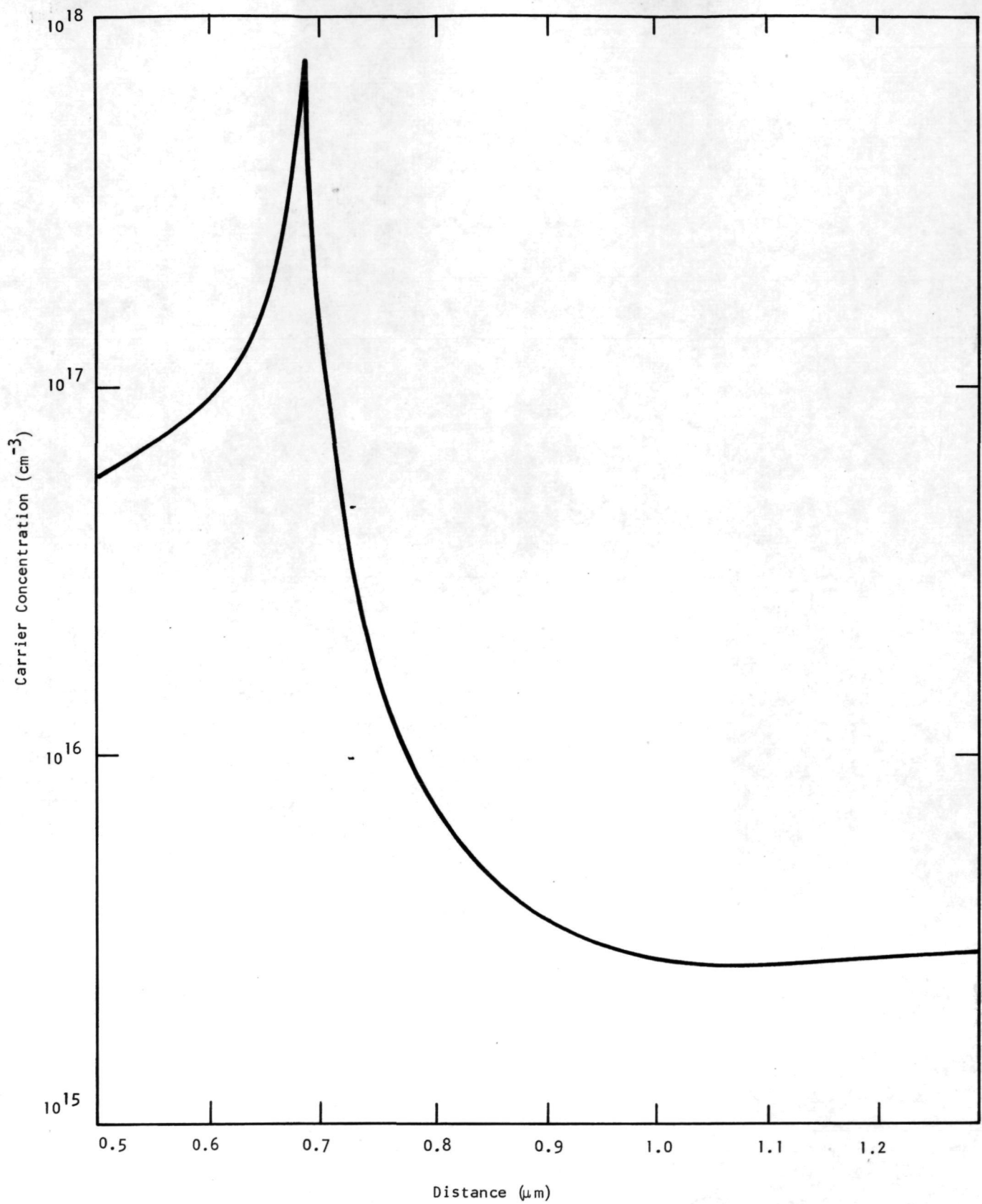


Figure 4 Doping Profile of Low-High-Low Read Diode Structure

Two approaches to solving this critical thickness control problem are possible. The first is to grow the layer to the required thickness. This would be a very low-yield procedure due to the extreme difficulty in maintaining such tight control over the growth. In addition, it could be difficult to form a good Schottky barrier to the as-grown layer, since growth terminates in a nonequilibrium vapor. Growth completion is not an instantaneous process; this uppermost layer would be a composition unlike that grown during equilibrium conditions and consequently could lead to the formation of a poor-quality metal-semiconductor contact.

A more attractive approach is one in which a postdeposition thinning process is employed to optimize the structure. In this method, the top layer is purposely overgrown and then thinned to the desired thickness. This method is made viable and very attractive by use of the anodic oxidation procedure described below. Without the anodic process, the thinning procedure is very difficult with the high-low structure because a reliable indicator, such as differential C-V profiling, samples the doping only as deep as avalanche breakdown will permit; therefore, unless a usually destructive pilot profile is established, e.g., by step-etching, the amount of surface high layer to be removed is not known. This problem does not arise with low-high-low structures where the small amount of overgrown, lightly doped surface layer is easily depleted as deep as the edge of the buried high layer. Supplied with knowledge of the amount of charge in the high layer (probably obtained by step-etching), one can estimate the amount of surface layer to be removed. A disadvantage of overgrowing the surface layer is that during the time of overgrowth, solid-state diffusion of the dopant species will tend to make the transitions between layers of greatly differing doping concentration less abrupt, and this may reduce device performance. However, if the anodic process is used, this disadvantage may be overshadowed by the tendency of the anodic process to produce a wafer of uniform breakdown voltage. This fact is borne out by experimental data for high-low structures, which show that for a relatively wide range of doping combinations, the optimum thickness of the

high layer results in nearly equal breakdown voltages. If it is recognized that an epitaxial slice will show variation in thickness and doping concentration, the distinct advantage of anodic oxidation for postdeposition thinning becomes apparent.

The anodic oxidation procedure for postdeposition thinning was originally used for the GaAs FET. Basically, the technique involves anodic oxidation of the GaAs slice in an appropriate electrolyte, followed by removal of the oxide in a chemical etch that does not etch the GaAs. In the case of Read diodes, the thickness of the oxide that is grown depends on both the applied voltage and the thickness and doping of the surface high layer. A voltage-limited condition is used.³ In practice, the applied voltage is chosen to be the same as the desired diode breakdown voltage, approximately 35 V for X-band diodes and 25 V for Ku-band diodes. When the high layer is too thick, this applied voltage is greater than the breakdown voltage of the layer so that current flows, allowing growth of an oxide. Oxide growth terminates when the excess voltage above breakdown is dropped across the oxide, since current no longer flows. The oxide is then stripped and the process repeated. The situation described above is illustrated in Figure 5(a) for a nonuniform GaAs slice in the early stages of anodic oxidation thinning. The doping profile of the slice is of the type shown in Figure 1(b). In this early stage of thinning, the electric field is distributed between the oxide layer and part of the high layer and does not extend into the low layer, as indicated in Figure 5(b).

Figure 6(a) represents the situation where part of the high layer has been optimized and part remains too thick. In the upper part of the figure, all the applied voltage is across the semiconductor so that no current will flow and an oxide is not formed. Full oxide growth is still observed in the lower part of the figure. The electric field distribution shown in Figure 6(b) for the central part of the slice is approaching the desired distribution shown in Figure 1(c)

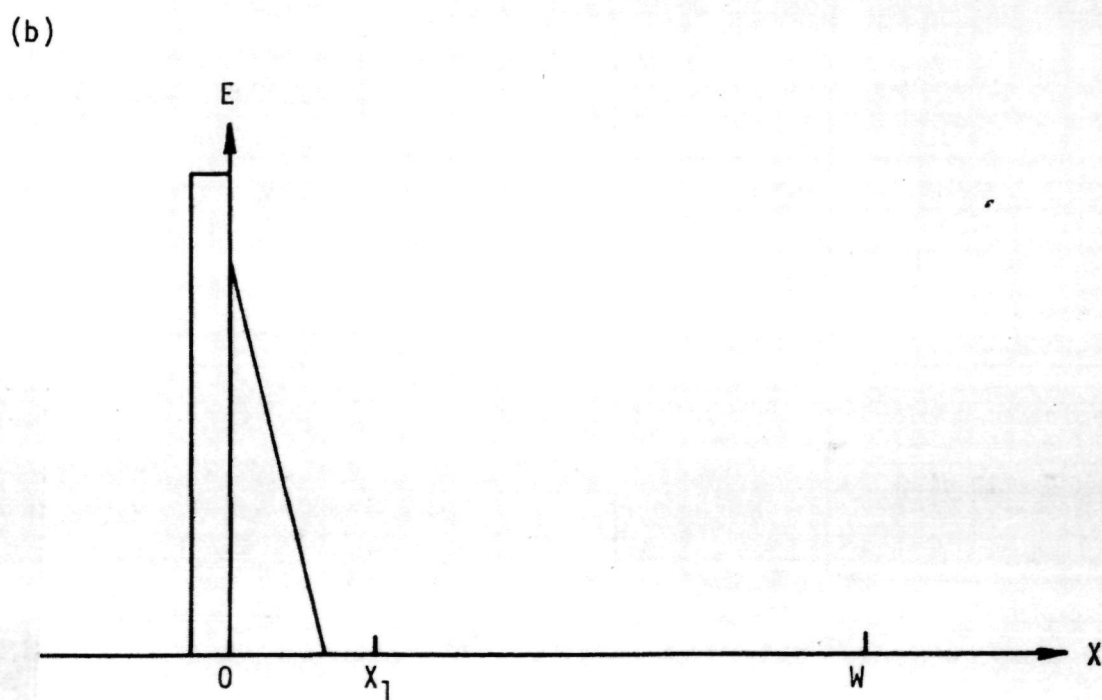
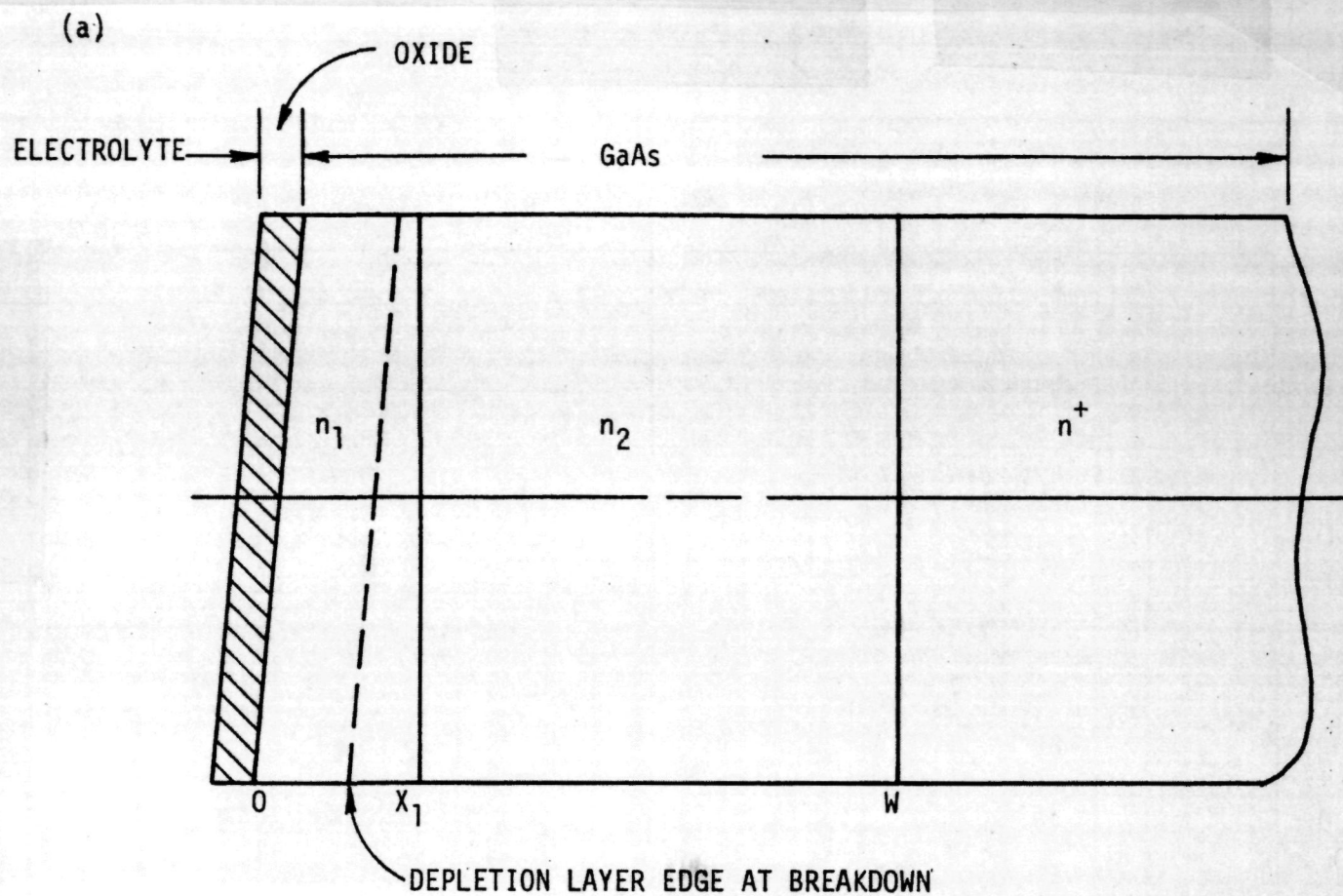


Figure 5 (a) GaAs Slice in Early Stage of Anodic Oxidation Thinning
(b) Electric Field Distribution Through Center of Slice

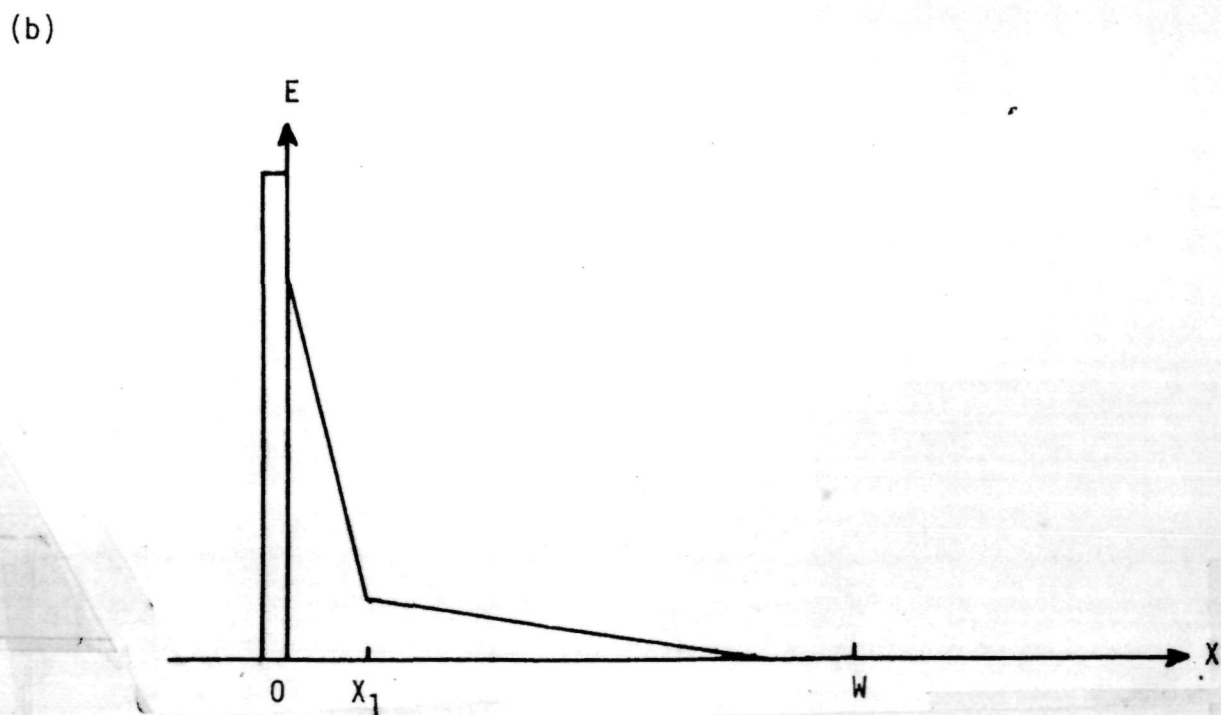
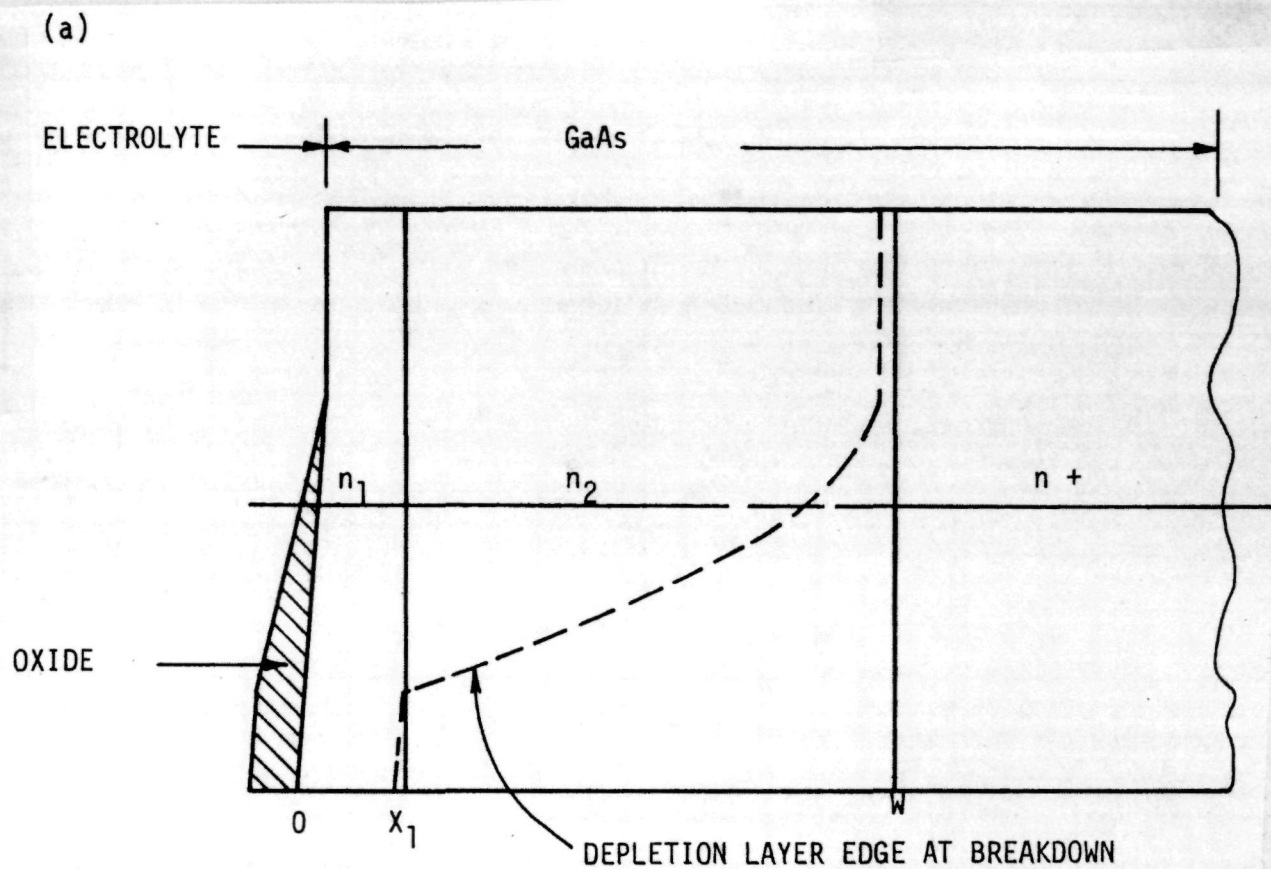


Figure 6 (a) GaAs Slice Near Completion of Anodic Oxidation Thinning
(b) Electric Field Distribution Through Center of Slice

By removing the oxide and repeating the cycle, the thickness of the high layer is adjusted to give a uniform breakdown voltage across the wafer. The oxide removal process is readily accomplished in situ by simply reversing the polarity of the applied potential and cathodically "lifting off" the thin oxide. This process evolves hydrogen gas, which must be allowed to escape from the wafer surface before reoxidation. A photograph of the experimental setup used for anodic oxidation is shown in Figure 7. The sample is carefully mounted in a holder so that only the front surface is exposed to the electrolyte. The electrolyte used for the anodic oxidation is an aqueous solution with sodium dihydrogen phosphate NaH_2PO_4 as the buffer ($\text{pH} = 4.5$). It has been found that the technique is sensitive to light and temperature. Therefore, the procedure is carried out in the dark with a chilled electrolyte. An automatic sequencer cycles the wafer between anodic and cathodic bias points, which are separately adjustable. For Ku-band devices the anodic potential of 18 to 24 V is applied for 8 to 10 seconds, and current is monitored. The current falls rapidly from its initial surge, which is reduced as the wafer approaches its correct thickness. Following the anodic phase, cathodic bias of 10 mA/cm^2 is applied for 10 to 20 seconds for oxide removal, after which the wafer debubbles for 10 to 20 seconds before the cycle is reinitiated.

Test results for wafers processed with anodic thinning have been compared with those for chemically thinned wafers and have shown no differences assignable to surface deterioration induced by the anodic/cathodic cycling process. Ideality factors under forward bias, reverse leakage currents, capacitance voltage data, and the microwave performance comparison diodes all sustain this conclusion.

The process has not been without difficulty, however. From a practical standpoint, the most annoying difficulty has been isolating the wafer so that only the surface is exposed to the electrolyte. A suitable

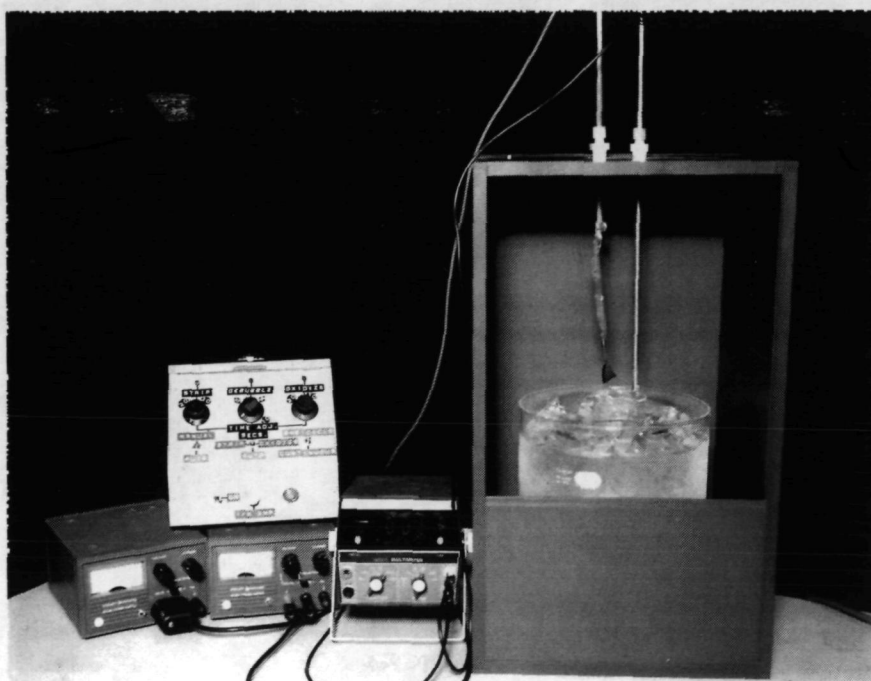


Figure 7 Anodic Oxidation Setup

system has been evolved in which a secure contact is soldered to the back of the wafer and the wafer is floated in photoresist on a flat holder with its front side periphery carefully painted to seal the edges. Operationally, the process results in a breakdown voltage greater than the cell voltage applied. The most likely explanation of this effect is the tendency for some oxidation to occur for cell voltage less than the breakdown voltage. For devices intended for X-band operation this fault is almost inconsequential, since a thicker oxide (removing more GaAs) can be grown with each cycle to properly thin the slice, and few oxidation cycles are required. However, Ku-band slices are approaching a practical limit for successful application of this technique on high-low structures because thinner oxides are grown with each cycle. During part of the contract period, a severe uniformity problem was encountered, and the many oxidation cycles necessary to reduce the initial oxidation current to a value indicative of process completion resulted in consistently overetched wafers. Since the change to a vertical substrate position was made, the uniformity has significantly improved, and only occasional overetching is observed. To further protect against the overetch problem, the criterion for completion of the cycling process has been changed from a 90% reduction of the initial surge current to only a 30% reduction. Although this results in a wider distribution of breakdown voltages on the completed slice, no cases of complete overetch have been encountered.

2. Fabrication Procedure

The plated heat sink fabrication process was developed at Texas Instruments to achieve rapid heat removal from high-power microwave devices.⁴ This technique is now widely used, particularly for IMPATT and Read diodes where most of the heat is generated near the Schottky barrier junction. The heat sink is plated directly to the Schottky barrier metal, and nearly ideal heat removal is achieved.

The procedure used at Texas Instruments to fabricate plated heat sink diodes is illustrated in Figure 8. The high layer (n_1) is initially thinned anodically to the desired thickness, and then a $0.6\text{ }\mu\text{m}$ thick Pt Schottky barrier is electroplated onto the epitaxial layer. Next, a thick Au heat sink is plated onto the Pt, and the substrate is thinned by lapping and etching to approximately $25\text{ }\mu\text{m}$ with the Au heat sink providing the necessary support. Electroplated Au, approximately $1\text{ }\mu\text{m}$ thick, is used as the back contact to the substrate. The mesas are defined using standard photolithographic procedures and etched with a bromine-methanol etch. The diodes can be probed at this stage, after which they are separated by sawing through the Au heat sink. The diodes are then mounted with AuSn solder in microwave test packages or on Au-plated Cu blocks for use in microstrip amplifier circuits.

It has been shown that the reactive contact afforded by the Au-plated back contact is adequate for avalanche devices. Should an ohmic back contact be desired, it is readily accomplished by alloying the Au-plated back contact with a drop of Au/Sn solder briefly at 340°C . The back contact is customarily left reactive unless detailed C-V data on the active Pt/GaAs Schottky contact is desired. With very heavily doped substrate material, the diode voltage with the Pt Schottky contact forward-biased (Au back contact reverse-biased) is typically 3 to 5 V, and the reactive contact to this material is a standard for comparison. However, in an effort to obtain superior epitaxial morphology, it was found that the use of more modestly doped substrates gave lower dislocation counts. Increasing the substrate resistivity specification accomplished the goal of a low substrate dislocation density and should, in theory, cause no significant increase in diode series resistance. It was observed that the forward voltage increased to the range of 5 to 10 V on wafers with reduced substrate conductivity. Serious question of the suitability of the reactive back contact to this substrate material was raised, and such devices have been made ohmic to avoid any influence from this modification. Although the back contacts

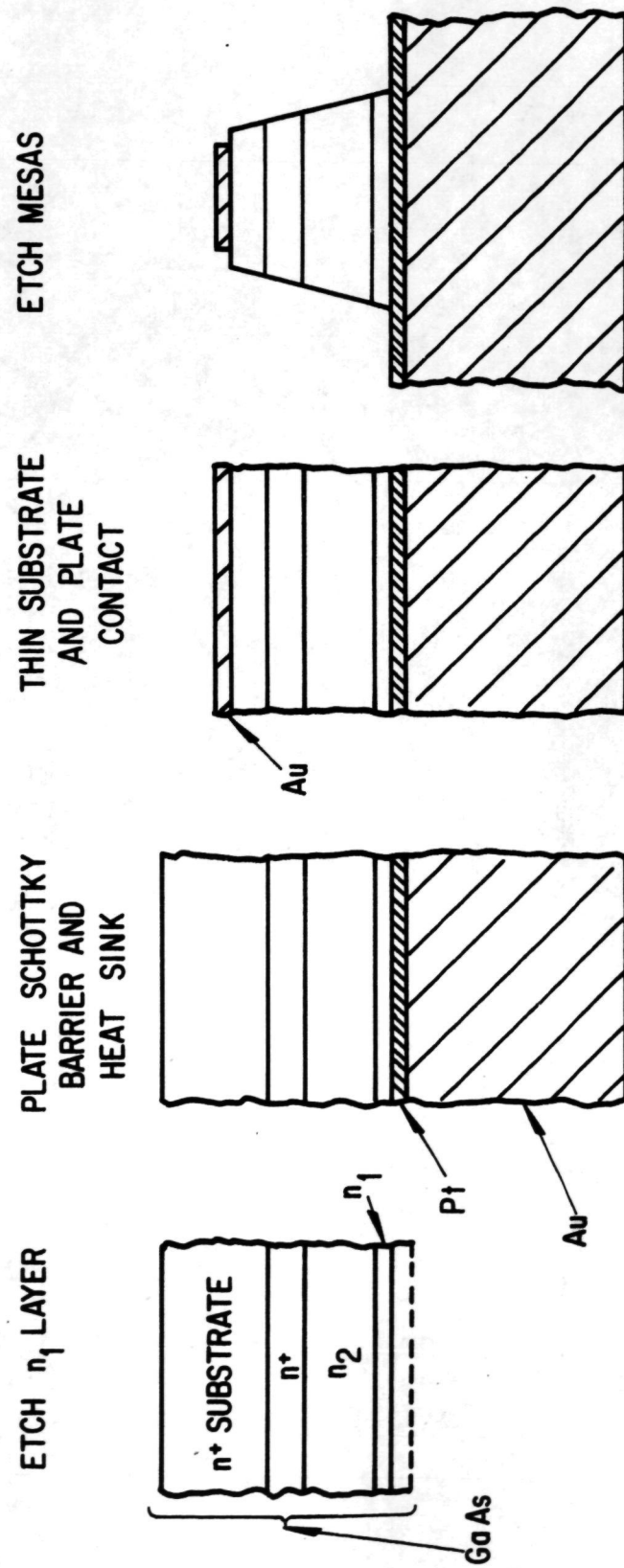


Figure 8 Plated Heat Sink Fabrication Procedure

were always made ohmic on these slices, diodes tested before and after the back contact was alloyed, showed little improvement with alloying of the back contact. An independent test of the diode series resistance was made by comparison with 25% efficiency X-band devices. The series resistance of these devices was measured using the DeLoach⁵ transmission technique. For this purpose, packaged diodes were etched to a size that would resonate at 8.3 GHz in 1.25 mm high reduced height waveguide with a 13 to 24 V reverse voltage applied. The high efficiency X-band devices gave a series resistance of 0.38 Ω . A similar lot of these devices with ohmic back contacts showed less than 10% change in series resistance. Ku-band devices from several slices were also tested. Although the Ku-band diodes had to be etched to significantly smaller diameter to achieve resonance using this technique, the average series resistance was only 0.37 Ω with a 25% standard derivation. No correlation between series resistance and slice performance was obtained for the Ku-band devices. From these measurements, it is concluded that the device structure does not contain an anomalous series resistance that is responsible for poor performance.

Another critical aspect of the device structure is its ability to transport heat away from the junction. This must be done through the heat sink and package assembly.

Photographs of a metallurgical section of GaAs Schottky Read diode soldered to a Cu block are shown in Figure 9. The mesa is approximately 160 μm in diameter by 25 μm thick. The heat sink is about 500 μm on a side after sawing and is 200 μm thick. The section was etched with a chromic oxide solution to remove smeared metal from the Au heat sink Cu block interface region.

The solder interface is approximately 10 μm thick and virtually void-free. Even though the Au plate on the Cu block goes into solution during the soldering operation, Cu is not dissolved due to the presence of a thin Ni

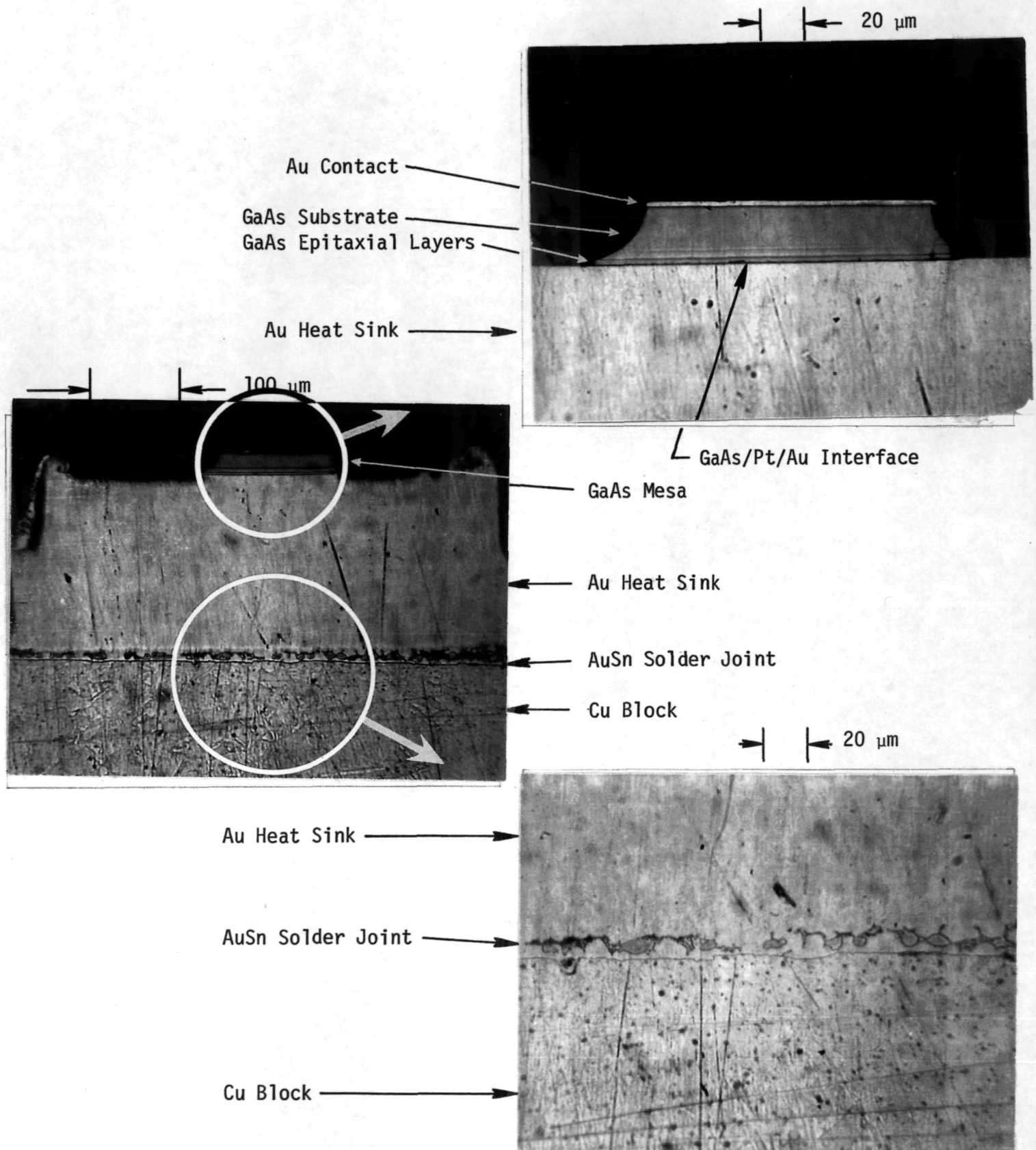


Figure 9 Metallurgical Section of a Plated Heat Sink Diode Soldered to Cu Block

barrier layer between the Cu block and the Au plate. The Ni layer cannot be resolved in the photograph, but there is a distinct line at the Cu/solder interface. Since the Au-plated heat sink goes readily into solution with the AuSn solder, the transition region is much less distinct in this case. Color photographs were found to be most helpful in determining the thickness of the solder joint and in showing the different intermetallic phases within this region. The dark features in the low magnification photograph of the solder region are intermetallic granules. They are clearly delineated in the magnified photograph of this region and are readily identifiable using color microscopy.

The etch rate of the chromic oxide solution for GaAs is conductivity-dependent so that horizontal lines at the etch steps can be seen on the mesa at the substrate/buffer layer and buffer layer/drift layer interfaces. The high layer is too thin for the other interface to be resolved.

The thermal resistance of a single-mesa diode with dimensions approximately the same as the diode of Figure 9 can be readily calculated from the diode geometry using these published values for thermal resistance: $K_{\text{GaAs}} = 0.4 \text{ W/cm } ^\circ\text{C}$, $K_{\text{Au}} = 3.0 \text{ W/cm } ^\circ\text{C}$, $K_{\text{solder}} \approx 0.5 \text{ W/cm } ^\circ\text{C}$, and $K_{\text{Cu}} = 4.0 \text{ W/cm } ^\circ\text{C}$. Five contributions to the thermal resistance are considered: laminar flow in the GaAs, spreading of the heat generated by the mesa into the Au heat sink, laminar flow in the solder joint, spreading of heat from the Au die into the Cu package, and spreading of heat from the package into the Cu heat sink. The resulting value for the total thermal resistance is 16.8°C/W for a $150 \mu\text{m}$ diameter single-mesa device, with over half of this value being due to spreading from the mesa into the Au die. By going to two mesas with the same total area on a single die of somewhat larger dimensions, the thermal resistance is reduced to 10.4°C/W , more than a 30% reduction. The reduction in thermal resistance achieved with two mesas is expected to be important for the final stage of the amplifier

A marker technique was used to check the heat flow resistance of fabricated devices. Packaged diodes were mounted in a portable heat sink and coated with an MBBA liquid crystal that undergoes a phase change to an isotropic light scatterer at about 60°C. This phase change can be viewed under a microscope while bias is applied, and by noting the input bias power at which the phase change occurs, the heat flow resistance may be computed. For recently completed devices, the heat flow resistance was found to be somewhat higher than is normally expected from plated heat sink devices. This technique of measurement allows determination of the isotherm at the critical temperature of the liquid crystal. Figure 10 shows such an isotherm that was observed on a Read device. A nearly circular mesa; its contact wire on top; the straight edges of the heat sink; and a portion of a second, unused mesa are visible in the photograph. The device is dissipating 2 W within its diameter of 150 μm . The ring surrounding the mesa is the isotherm that separates the isotropic liquid crystal toward the interior of the ring from the nematic liquid crystal toward the exterior of the ring. Note that the isotherm appears off-center toward the right-hand side of the photograph. The nonsymmetric isotherm was observed in several Read devices that were examined.

IMPATT devices that have a flat doping profile show an isotherm that is located symmetrically around the mesa periphery. The nonsymmetric isotherm observed on the Read devices is caused by a nonsymmetric generation of heat across the device mesa and is believed to be a consequence of a nonuniform high-layer thickness. To support this hypothesis, devices from a Read slice with known thickness gradient were examined and in every case showed the isotherm shifted off-center from the mesa in a direction opposite to the thickness gradient.

Although thickness gradients can reduce device yield because devices of appropriate breakdown voltage can be obtained only at a specified thickness, it is surprising to find that thickness gradients across a mesa diameter can



Figure 10 Optical Photograph of a Read Diode Mesa Coated with Liquid Crystal, Showing the Nonsymmetric Isotherm Indicative of Nonuniform High-Layer Thickness

reveal themselves in the manner that has been demonstrated. Poor microwave performance because of the nonuniformity is very likely, since it renders only the thinnest edge of the mesa active and the remainder parasitic. As an upper bound, the thickness difference across a 150 μm diameter mesa has been no more than 150 \AA in the devices prepared under this contract. These experiments revealed inadequate circulation of reactant gases over the substrate during epitaxial growths. The fault was immediately corrected, and substrate orientation changed from along the reactor gas flow direction to the normal gas flow or vertical direction. Subsequent wafers have shown a marked improvement in uniformity, reflected principally in the ease with which the high layer is thinned, and have not displayed the nonsymmetric isotherms during heat flow resistance measurements.

The liquid crystal technique for measuring the heat flow resistance still results in a thermal resistance of 20 to 25°C/W rather than the 16 to 20°C/W expected. Device sections indicate that the heat sink is void-free and that the solder joint is well compressed. No cause for the high values has been found. However, measurements of Gunn devices on Ag heat sinks have also shown somewhat high values, and it is possible that the result is due to an unknown systematic error. The high thermal resistance will have to be addressed to assure the maximum device reliability, but for breadboard amplifier design and device evaluation, the measured values are sufficiently low that no performance degradation is anticipated.

3. Evaluation

After mesa diodes have been fabricated on the plated heat sink, several stages of evaluation are performed. These include obtaining a map of the reverse-breakdown voltage of each slice processed, a check of forward I-V characteristics, an examination of the cosmetic appearance of the mesas

and exposed Pt which is a replica of the initial epitaxial GaAs surface, and a sampling of the doping profile of the slice using selected mesas. All these tests can be performed on the slice prior to separation of the individual mesas on their plated heat sinks. Following separation of the individual mesas, selected diodes are soldered into a package and tested for microwave oscillator performance.

These extensive evaluation procedures ensure that diodes used in the amplifiers are capable of the high performance demanded of them, and only those slices that qualify are used in the transmitter. Additional details of the evaluation procedures are given below.

a. Voltage Mapping

When the mesas are etched, a regular array of diodes is delineated on the plated heat sink. The diodes are individually contacted by a probe that can be stepped across the slice automatically in units of diode separation. The automated stepping allows probing of every diode in a short time.

Several aspects of the I-V characteristic are observed. The forward voltage (i.e., bias applied of such polarity as to forward-bias the active Pt-GaAs Schottky barrier) at a few milliamperes should be less than 5 V unless a low dislocation density substrate of slightly increased resistivity is used. About 0.7 V of the forward voltage is dropped across the Pt Schottky barrier. The remainder is dropped across the back Au-plated contact, which is, of course, a Schottky barrier in reverse bias. Since the back contact is made on heavily doped substrate material, its reverse voltage should be low. Abnormally high forward voltage usually indicates a problem with the process run such as a poor Au-plated back contact or an extremely thin mesa such that contact is made to the buffer layer.

The reverse I-V characteristics of the Pt-GaAs Schottky-Read diode typically show a relatively soft reverse breakdown voltage. Other information as to the nature of the reverse characteristic is often recorded because of the wide variations observed. The voltage map is extremely useful, since it allows selection of diodes with proper breakdown voltage (i.e., thickness of the surface high layer) for further microwave testing.

b. Oscillator Performance

Diodes of appropriate breakdown voltage are selected from the voltage map and soldered into a special package, as is necessary at Ku-band frequencies for initial microwave oscillator testing. To minimize package shunt capacitance, the pedestal and screw mounting of the Met Ceram 60-7090 package was used with the ceramic and flange of the Met Ceram 60-1300 package. This combination has been found to be effective in removing heat while maintaining sufficiently small package parasitics to allow Ku-band operation of the diodes below any package resonance. Further, the package is convenient to use in the test fixture. The back contact of the soldered diode and the flange of the package are connected by cross-bonding a pair of $12\ \mu\text{m} \times 125\ \mu\text{m}$ Au ribbons.

Figure 11(a) is a schematic of the waveguide hat cavity used for oscillator testing. It is a scaled version of the cavity used extensively at X-band. A hat 3 mm high and 7 mm in diameter has been found to be suitable for most diodes operating near 13.5 GHz. Bias is applied through the anodized aluminum feedthrough, and the diode heat sink is water-cooled.

A constant voltage power supply is used for the dc source. A series resistor of 0, 50, 100, or 300 Ω is put in series with this supply to bias the diode as indicated in Figure 11(b). Although many devices will operate without the inclusion of any series resistance, the 100 Ω value is customarily used to avoid unnecessary tuning-induced transients that might cause a diode to fail.

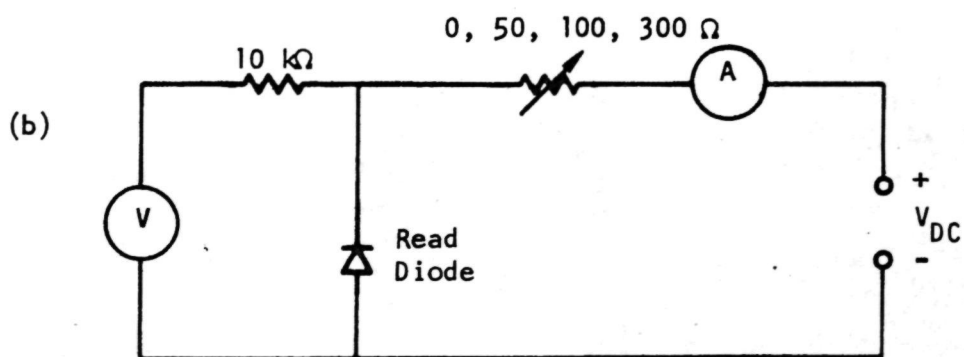
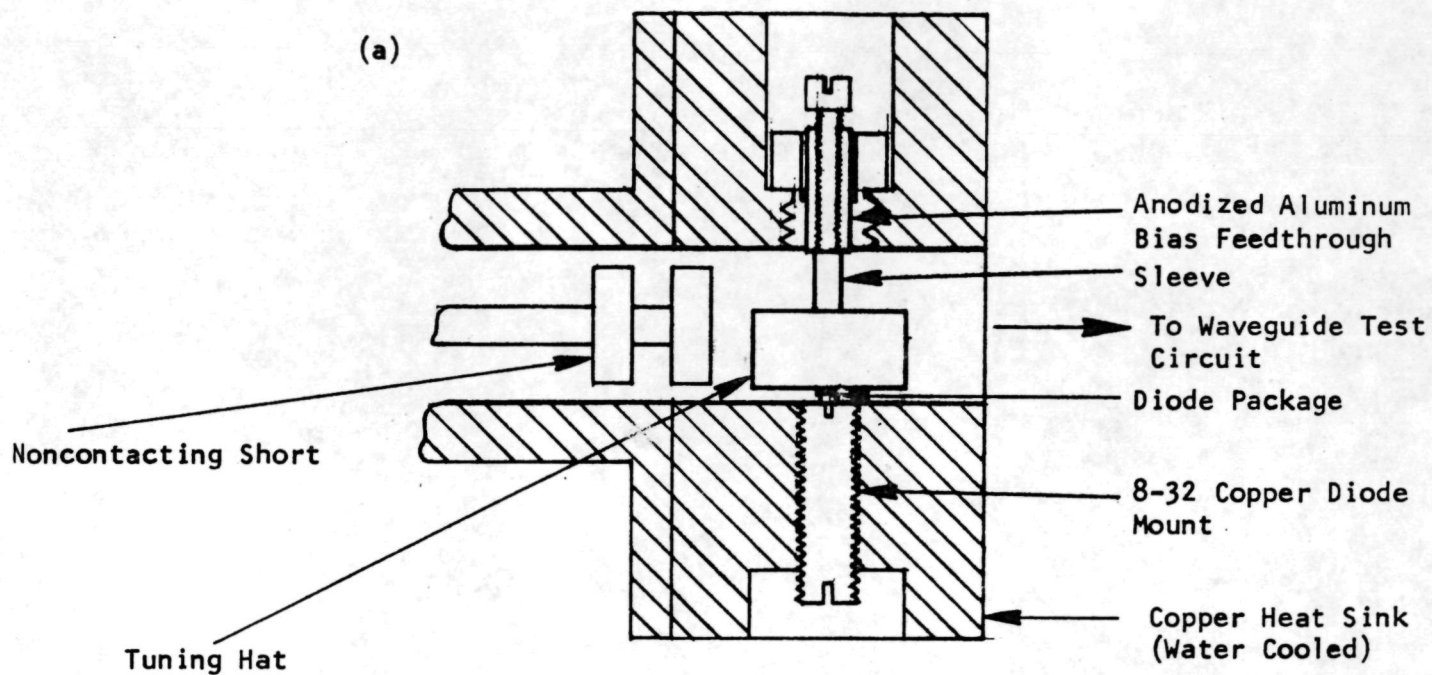


Figure 11 (a) Diode Waveguide Cavity
(b) Bias Circuit

With bias applied to the diode, a wide range of load impedance may be presented to the diode by varying the position of the noncontacting short and the depth and position of a slide screw tuner attached to the output port of the waveguide cavity. The Read diode response to the load conditions presented by this configuration does not always lead to smooth tuning, and the devices commonly jump into their high-efficiency mode of operation. This mode is characterized by a high current, low voltage dc operating point. Consequently, the $100\ \Omega$ dc load line of the bias circuit lets the diode fall to a state of lower dc power dissipation if it drops out of high-efficiency oscillation. To minimize transient effects that may occur during tuning-induced dropout, the length of the bias line between the series resistor and the bias feedthrough is kept short, and as little capacitance as possible is allowed to shunt the diode.

In general, the Read diode is found to be much more tolerant of tuning-induced transients than its flat doping profile IMPATT counterpart. Nonetheless, care is always exercised in tuning the diodes. The procedure involves first tuning a diode at relatively low bias levels to obtain approximately optimum positions of the noncontacting short and slide screw tuner. Bias is then increased slowly, and minor tuning adjustments are made until either power or efficiency saturation is obtained.

Figure 12 shows the oscillator performance of a high efficiency Read device operating near 13.6 GHz. The diode is from wafer 16272-136, whose doping profile is shown in Figure 13. The available output power increases smoothly with input power over the range shown. There is a maximum in efficiency of 23.5%. Further increase in bias can yield more power, but the efficiency would continue to fall until, ultimately, the power would saturate or reach a maximum. The operating voltage is shown in parentheses beside the data points on the figure. As with most Read devices, the operating voltage varies slowly with current, and negative differentials are not uncommon. Should the diode drop out of oscillation at the highest operating levels, the voltage would increase 6 to 10 V along the $100\ \Omega$ bias load line.

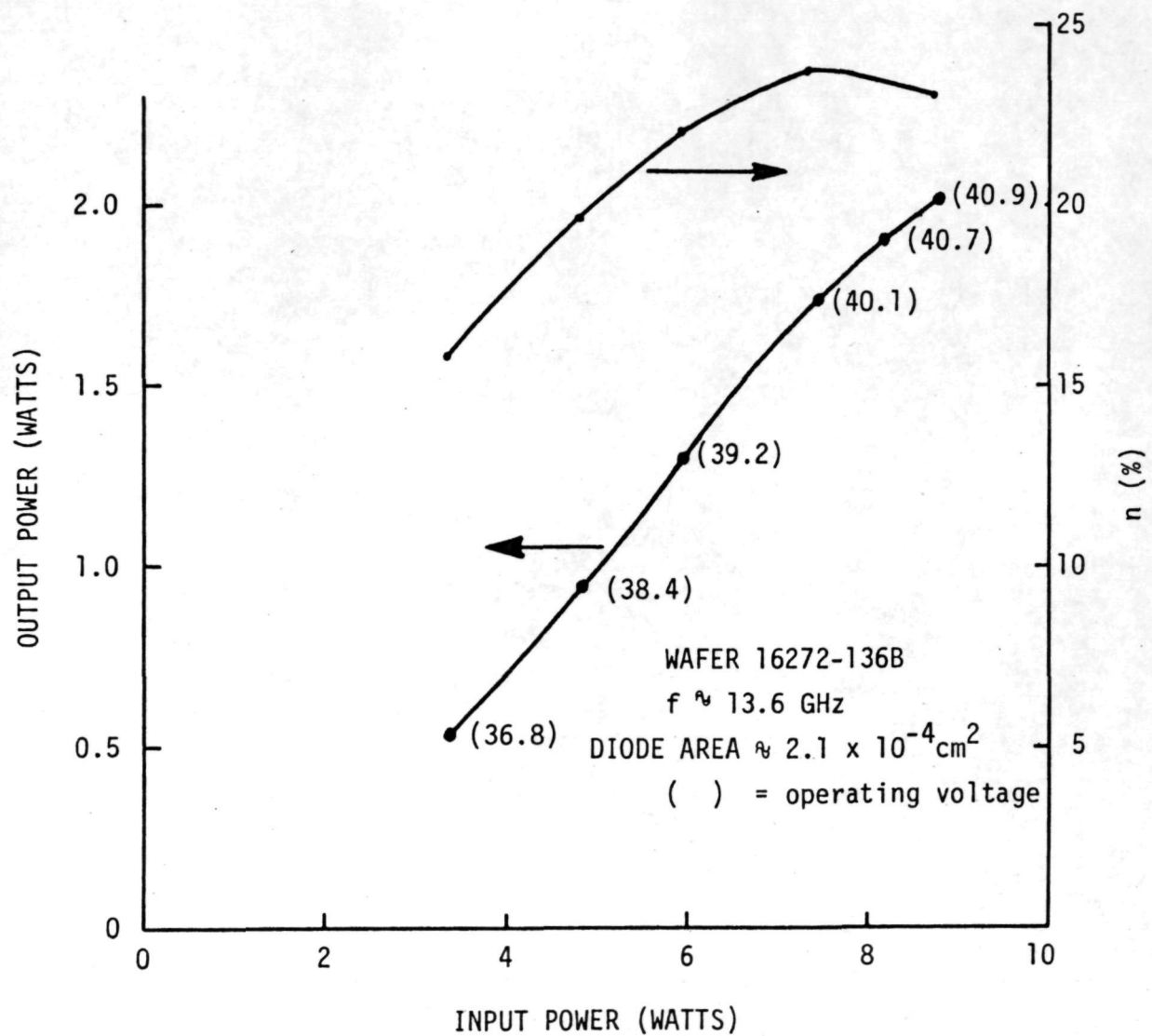


Figure 12 Output Power and Efficiency of a Ku-Band Read Diode Operating at 13.6 GHz

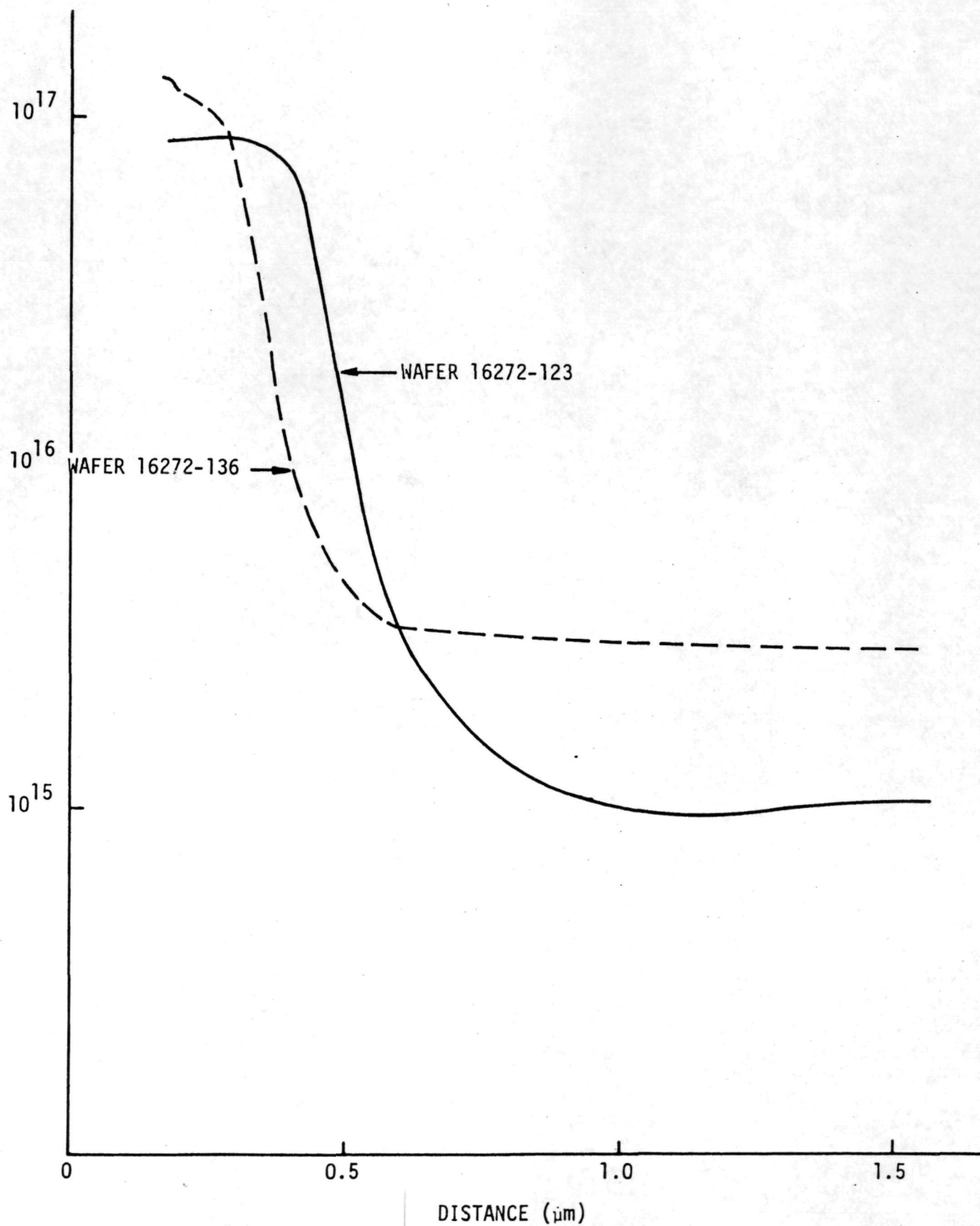


Figure 13 Doping Profiles of Ku-Band Read Slices

A peak power of 3 W at 20% efficiency and a maximum efficiency of 24.3% with 1.8 W of power have been observed at Ku-band through these oscillator tests. The results obtained by oscillator testing generally yield diodes that perform best at lower frequencies in microstrip circuits. By changing the tuning hat used in the waveguide circuit, the oscillation frequency can be changed. However, the best performance in the waveguide oscillator circuit is still observed at a higher frequency than is optimum for microstrip amplifier circuits. To further characterize this effect and also to test the fabrication process, a flat profile IMPATT slice suitable for Ku-band devices was selected for processing.

c. IMPATT Fabrication and Testing

Since the only difference in the process for Read and IMPATT devices is in the initial thinning of the surface layer, the IMPATT slice was cleaved in half and the surface of one of the halves prepared as if it were a Read slice while the second half was prepared in the usual IMPATT manner. Therefore, one half was oxidized at 80 V and the oxide stripped three times, typical of Read slice preparation. The other half was chemically etched two minutes in a 1 M NaOH:H₂O₂ solution as is the usual IMPATT procedure. Further processing on the two slices was identical. Both slices yielded devices with abrupt avalanche conduction, and further comparison in microwave tests showed no significant difference between the two process runs. These tests strongly suggest that the anodic thinning procedure does not influence device performance.

Initial microwave testing of the IMPATT devices showed only 4% efficiency with 400 mW oscillator power at Ku-band. The devices showed an anomalous tuning character in the waveguide hat circuit with extreme difficulty in obtaining the higher frequencies. A problem with the package was suspected, and an experiment was designed to test for package resonance. Packages were prepared by connecting one, two, and four 12 x 125 μ m Au straps placed symmetrically from the package flange to the pedestal and back to the flange.

These packages were mounted at the floor of the waveguide and connected across the waveguide height by a 3 mm diameter post. Reflection minima were observed at frequencies of 12.4 GHz, 14.4 GHz, and 15.5 GHz for the one, two, and four strap packages, respectively. With a device bonded in the package, its capacitive susceptance would significantly increase the resonant frequency. The resonant frequency that was measured indicates that four straps are sufficient to extend the combined package resonance above the device operating frequency as desired. Two straps have been employed for most of the Read work, and even this should be acceptable. However, when the IMPATT devices were bonded with four straps instead of two, the efficiency increased to nearly 7% and the power increased to 700 mW with smoother tuning than could be achieved with a pair of straps. Such dramatic improvement has not been observed with Read devices.

The IMPATT devices were ultimately tested in microstrip oscillator circuits and showed nearly 7% efficiency with 1 W output at 13.4 GHz. This performance is comparable to the waveguide tests and is typical for IMPATT devices. Processing the IMPATT slices has not completely eliminated the possibility of a fabrication problem, since the ultimate 12% efficiency was not achieved. However, the IMPATT performance was good and does not indicate that the processing technique should be suspected as limiting device performance.

d. Doping Profiles

When a diode with somewhat high breakdown voltage and low leakage current is encountered, the Au back contact can easily be converted to an ohmic contact by simply alloying the Au back contact with Au/Sn solder at 340°C. The mesa is then suitable for differential C-V doping profile analysis. Doping profiles are also obtained at the pre-processing stage and the post-microwave testing stage when the diode is packaged. Pre-processing doping profiles are customarily obtained by plating Au dots through holes in photoresist on a step-etched portion of a slice. These profiles are obtained

rapidly and used primarily to monitor reactor growth data. Diodes that show extremely good performance are usually profiled in the package. However, profiles obtained from mesas with ohmic back contacts are the most accurate. Selected doping profiles obtained from slices grown early in the program that have shown in excess of 20% efficiency at Ku-band are shown in Figure 13. For both of these slices the transition from high to low doping is essentially complete in less than 2500 Å. Note also the flatness of the doping concentration in the lightly doped layer. This quality has been observed to be common to several slices of high efficiency. It should also be apparent from the profiles shown in Figure 13 that the exact doping levels of the high and low layers are not extremely critical, at least for obtaining oscillator efficiencies over 20%.

Successive slices grown with doping profiles similar to those of Figure 13 have not, in general, been suitable for the amplifier. Although the single-mesa qualification tests of the devices show good performance, the frequency is typically low. Device profiles were used that increased the drift layer doping to 10^{16} cm^{-3} . These devices consistently oscillated at higher frequencies and show best operation in the microstrip circuits at the desired frequency. Oscillator efficiency of only 12 to 18% has been achieved with the slices of more highly doped drift layer. Increased drift layer doping increased the frequency as expected; however, if the high layer doping is kept constant, it also results in a lower high-low ratio and reduced efficiency, as expected in theory. A concurrent increase in high layer doping should then result in increased efficiency. However, it also increases the maximum field strength and results in enhanced tunnel injection. This injected current does not have the favorable phase delay of avalanche and may therefore tend to reduce efficiency. Most of our data indicate that this mechanism is actively limiting device efficiency. Since the low-high-low structure will reduce the peak field in the device while retaining the avalanche over a narrow region, it offers an attractive opportunity for improvements; this is discussed in

Section IV of this report. Figures 14 and 15 show 13 high-low doping profiles from slices that have shown modest power and/or efficiency at Ku-band frequencies when tested in the waveguide hat circuit. These slices are selected from a large group to give an indication of the variety of combinations of doping level that have been fabricated into devices under this contract. The results of microwave testing for these profiles are given in Table II. This collection of profiles indicates a rather broad combination of high and low doping levels that yield good microwave performance. A common characteristic which these wafers share is a drift doping level with slope less than or equal to zero. Although a firm connection with theory has not been established, a large body of empirical data exists to support the necessity of this profile characteristic in achieving good performance. The operating current at which the maximum power is obtained is loosely correlated with the minimum doping in the drift layer. This occurs because of a dynamic space charge limitation that prohibits collection of the injected charge bunch for larger currents. Finally, note that although the profiles represent a large variation in doping, the 10 mA breakdown voltage and operating voltage reflect a much smaller variation. It is the variation of high layer thickness that causes the relative constancy of device voltage with profile changes and shows why the anodic thinning process is so ideally suited to optimum slice preparation.

D. Reliability Considerations

Since IMPATT and Read diodes operate at relatively high temperatures, consideration must ultimately be given to the effect of these temperatures on long-term device reliability. Two mechanisms will impact the long-term reliability of the current device structures:

- (1) The reaction of Pt and GaAs that results in compound formation and displacement of the Schottky barrier, and
- (2) Au diffusion through the Pt Schottky barrier with continued diffusion of Au into the GaAs active region.

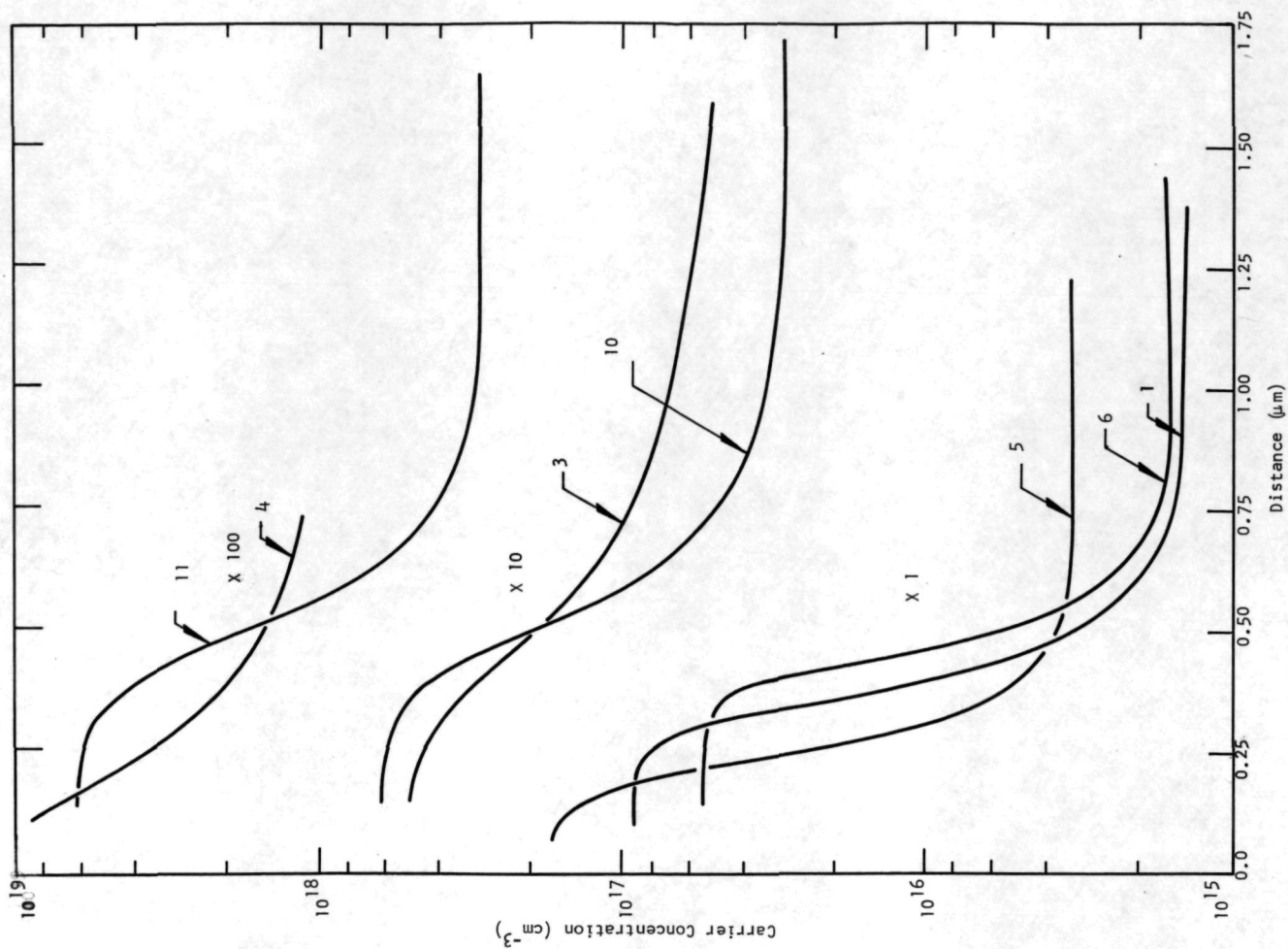


Figure 14 Doping Profiles of Ku-Band Read Slices

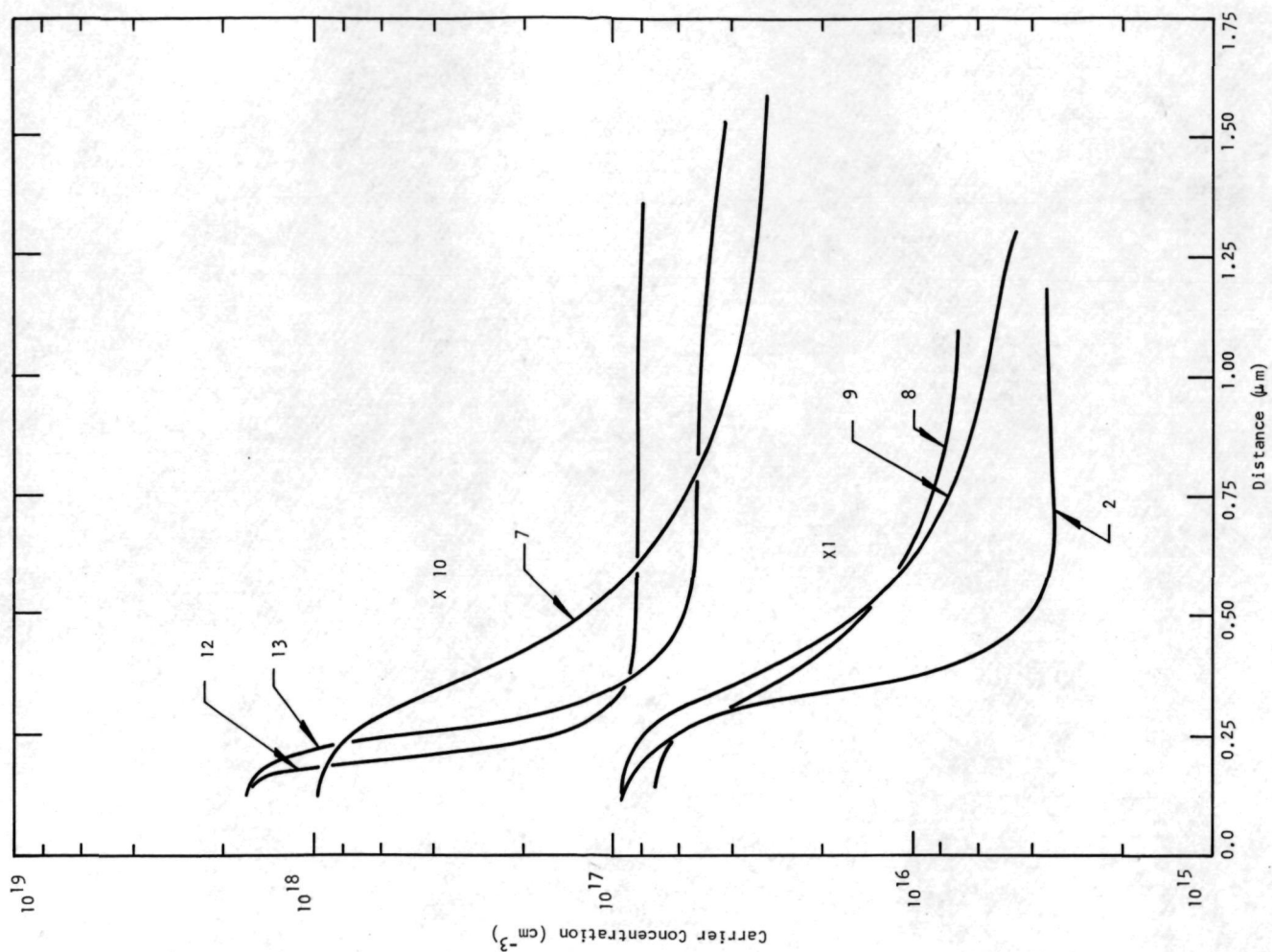


Figure 15 Doping Profile of Ku-Band Read Slices

Table II

Performance Comparison of Single 150 μm (Nominal) Diameter
Diodes from Various Wafers

<u>Profile</u>	<u>Slice</u>	<u>P_{rf} (W)</u>	<u>η_{Max} (%)</u>	<u>f (GHz)</u>	<u>I_{Max} (mA)</u>	<u>V_S¹ (Volts)</u>	<u>V_B² (Volts)</u>
1	76c1080	1.6	19.6	12.6	196	44.1	27.9
2	76c1081	2.2	16.1	13.0	354	38.8	27.0
3	76c1100	1.7	12.8	13.7	358	37.4	21.8
4	76c1144	1.7	11.2	13.4	393	40.8	29.0
5	76c1024	1.7	19.2	13.7	200	37.5	21.4
6	76c2025	1.4	19.2	12.8	209	38.3	18.8
7	76c2051	1.8	16.5	13.2	285	37.3	21.9
8	76c2053	2.0	17.0	13.9	308	38.2	22.5
9	76c2055	2	17.3	14.0	300	42.0	26.3
10	76c2056	1.8	16.4	13.1	269	42.1	22.8
11	76c2059	1.1	12.6	12.6	202	42.1	23.5
12	76c2069	2.1	14.4	12.9	396	37.5	26.5
13	76c2075	1.9	16	14.7	326	37.4	26.3

1. V_S is measured at peak output power
2. V_B is measured at 10 mA bias current

Both of these failure mechanisms can be halted by incorporating a W diffusion between a very thin Pt Schottky barrier and the Au heat sink. In fact, the utility and effectiveness of this barrier has been demonstrated by Texas Instruments.

However, because of the difficulty in obtaining the desired goals of this contract, it was decided that the introduction of any possible additional complications into the fabrication procedure would create extra variables that would only be directed to long-term reliability improvements in any case. Since the reliability problems were recognized, the standard thick Pt process was retained.

SECTION III

TRANSMITTER DESIGN

A. Introduction

The purpose of the microwave integrated circuit (MIC) work performed under Contract No. NAS5-20894 was to demonstrate the feasibility of developing a Ku-band solid-state spacecraft transmitter. The transmitter was to consist of GaAs IMPATT and Read diodes operating in a microstrip circuit environment to provide amplification with a minimum of 63 dB small signal gain and a minimum compressed gain of 57 dB at 5 W output. Other performance specifications are listed in Table I. Consistent with the plan specified in the RFP, the program consisted of two phases. The first phase ended with the delivery of a breadboard transmitter module. Since several problem areas were identified during Phase I of the contract, a contract modification was made at the completion of Phase I to redirect the program effort toward finding solutions to these problems. At the end of Phase II, an improved breadboard transmitter was delivered in place of the two spacecraft transmitters originally scheduled.

This section of the report covers the design and performance of the Phase I breadboard module, including the microstrip circuit and circulator optimization, preamplifier development, power amplifier development, and dc-to-dc converter design. In addition, several critical design problems uncovered during Phase I are discussed, and the design changes incorporated into the improved breadboard transmitter module delivered at the end of the contract are described.

B. Phase I Accomplishments

In this subsection the design and performance of the individual components leading to the construction of the Phase I breadboard transmitter module are discussed. These components include the MIC circulator, preamplifier, power amplifier, and dc power supply.

1. MIC Circulator

A high performance microstrip circulator is a prerequisite for the design of a reflection-type amplifier. In addition to separating the input and output signals, the circulator can also be used as an isolator, when properly terminated. A high degree of interstage isolation will be required to minimize the undesirable coupling between stages and to reduce the tendency for spurious oscillations to occur when high-gain amplifier stages are cascaded.

The material selection for the circulator design was based on the following criterion:

$$\frac{\gamma 4\pi M_s}{f} \sim 0.5 ,$$

where γ is the gyromagnetic ratio ($= 2.8 \text{ MHz/Oe}$), f is the frequency of operation in megahertz, and $4\pi M_s$ is the saturation magnetization in gauss. TRANS-TECH TT1-390 ferrite with a $4\pi M_s$ of 2150 gauss can readily satisfy this design criterion and was used for the circulator fabrication.

The design procedure outlined by Fay and Comstock⁶ was used to arrive at an optimum microstrip circulator design. For simplicity, a single quarter-wave transformer was used for broadband impedance matching. The disk diameter, the characteristic impedance, and the length of the matching transformer, along with the bias magnetic field, were optimized with respect to the bandwidth, insertion loss, and isolation. As a result of this intense investigation, a wideband MIC circulator design was achieved at Ku-band frequencies. One of the circulator designs covers the frequency range from 11 to 16 GHz, while the second unit (with a slightly smaller disk diameter) can be used from 12.5 to 17 GHz. Generally, these circulators exhibit an insertion loss between 0.5 and 0.7 dB (including connector and transmission line losses), an isolation greater than 20 dB, and VSWR less than 1.2. An all-ferrite substrate (TRANS-TECH TT1-390) was used for the circulator pattern.

Broadband matching of the circulator junction to the $50\ \Omega$ transmission line was accomplished by placing a magnetic material on top of the circulator disk, in addition to the bias magnet placed beneath the ground plane. Thus, the dependence of the characteristic impedance of the microstrip transmission line on the bias field configuration was effectively utilized for broadbanding the circulator Y junction.

A single quarter-wave transformer was initially planned as the circuit element for broadband matching the circulator junction; however, the dc fringing field of the circulator bias magnet provided an additional degree of freedom in accomplishing the match. The fringing field of the bias magnet can cause the characteristic impedance of the quarter-wave length transmission line to change along the direction of propagation of the EM field. The amount of change depends on the interaction between the rf magnetic field and the component of dc magnetization parallel to the direction of propagation, since this interaction changes the value of the effective permeability of the ferrite, resulting in a change in the characteristic impedance.

Figure 16 shows the test fixture for the Ku-band circulator. The performance characteristics are shown in Figure 17. This circulator uses a 0.5 mm (20 mil) thick, TT1-390 ferrite as the substrate and has a disk diameter of 4.06 mm (0.160 inch). A single quarter-wave transformer with a characteristic impedance of $31.6\ \Omega$ (with the ferrite demagnetized) is used for impedance matching. The circulator is biased with a SmCo permanent magnet [6.35 mm (0.250 inch) in diameter and 3.18 mm (0.125 inch) thick] located beneath the ferrite disk resonator. The optimum field has been achieved by adjusting both the bias field and the "matching top" configuration discussed earlier. A 0.25 mm (10 mil) thick shim in combination with an iron matching top with the same diameter as the circulator, i.e., 4.06 mm (0.160 inch), and 2.54 mm (0.100 inch) thick, yields the microwave performance shown in Figure 17. This circulator design has been incorporated into the construction of the multi-stage MIC amplifier to be discussed later. Excellent results have been obtained.

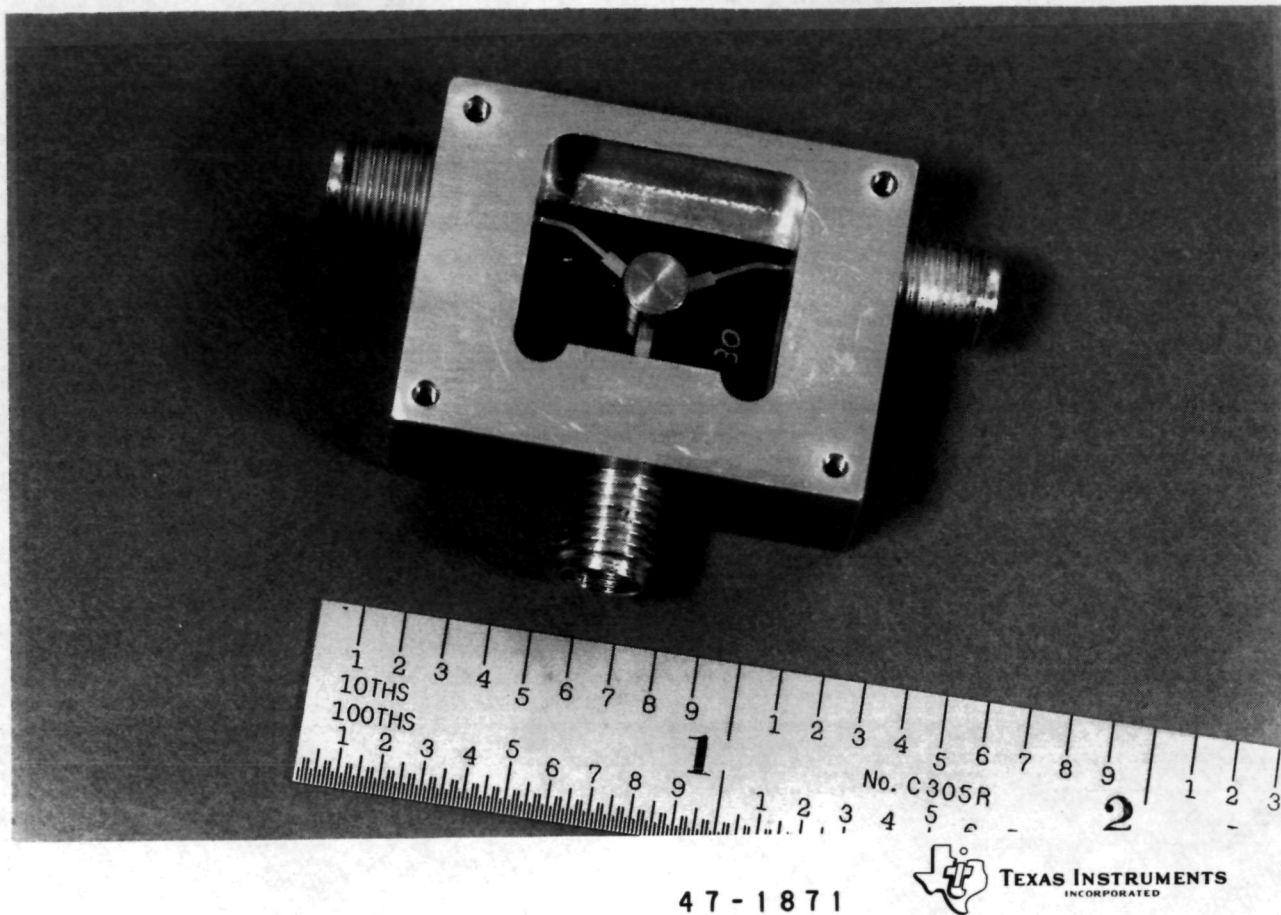


Figure 16 Photograph of a Test Fixture for a Microstrip Circulator

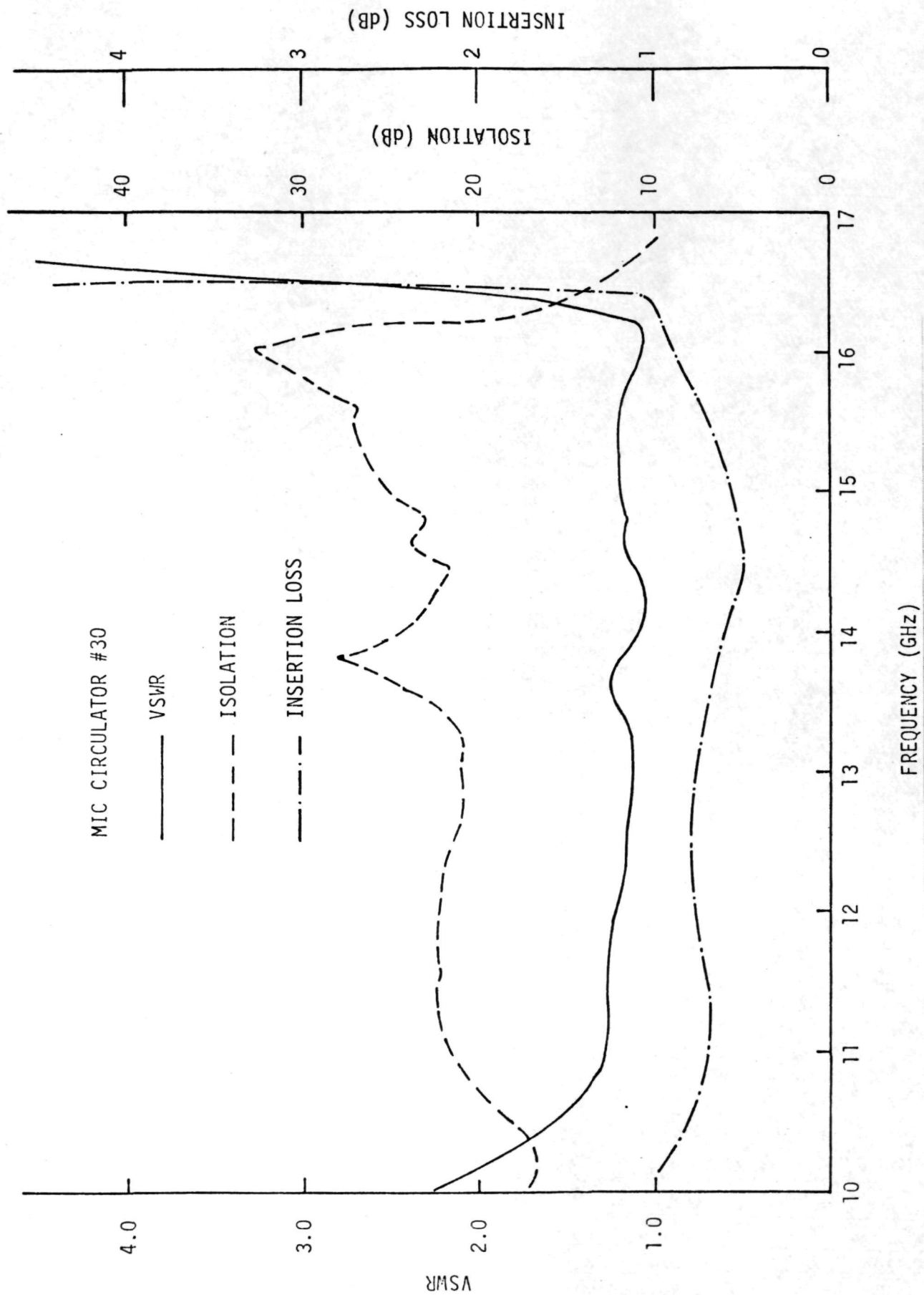


Figure 17 Characteristics of an X/Ku Band MIC Circulator

2. Preamplifier Design and Performance

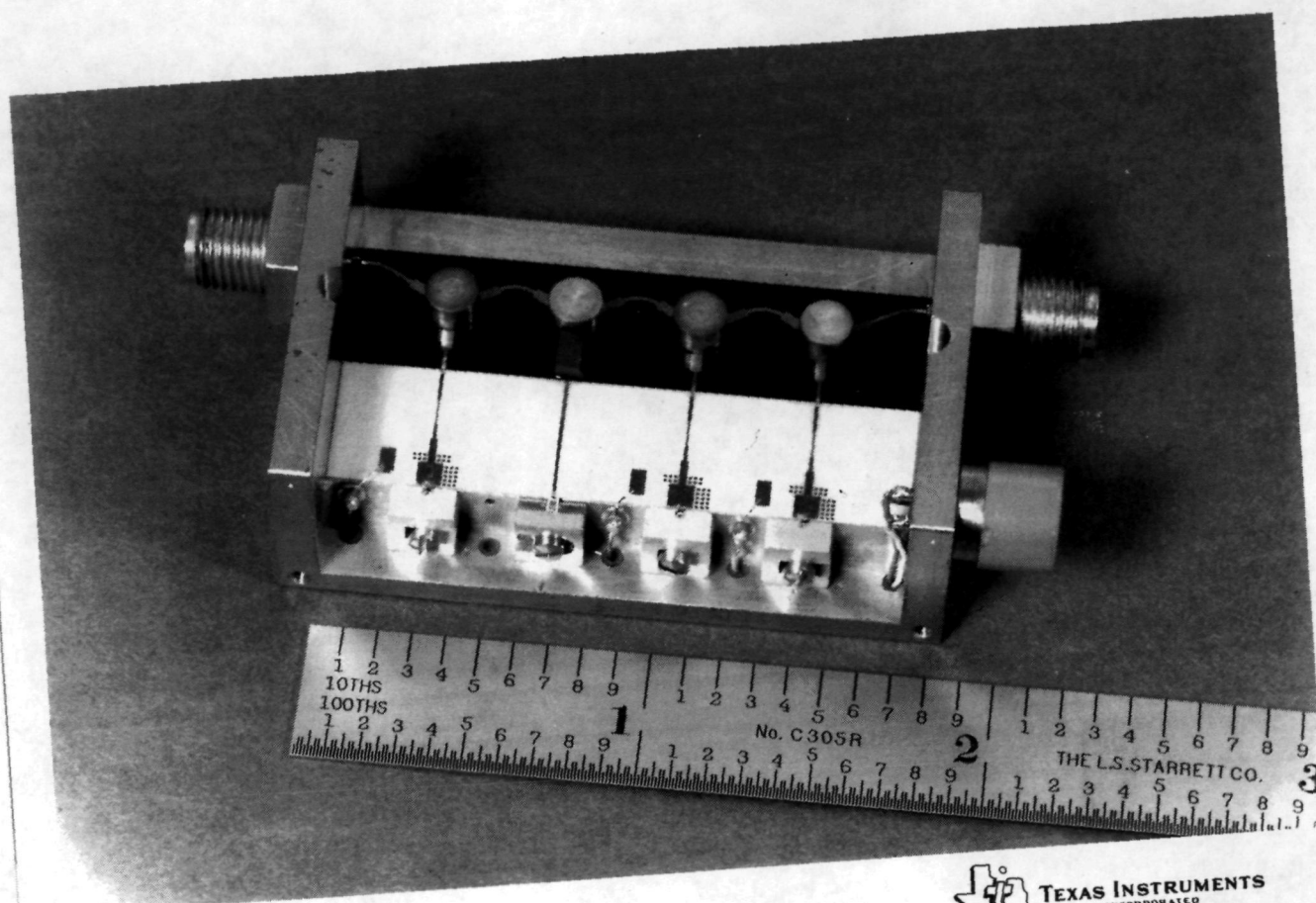
To facilitate testing and tuning, the transmitter has been separated into two amplifiers. The preamplifier consists of three GaAs IMPATT amplifier stages in cascade. The power amplifier utilizes high-low GaAs Schottky-Read diodes as the negative resistance elements for increased powers and efficiencies. The preamplifier is to provide a small signal gain of ~ 35 dB at an output power of 15 dBm over the design frequency range of 13.4 to 13.65 GHz.

Prior to construction of the multistage integrated preamplifier, GaAs IMPATT diodes (flat profile) were used in various single-stage microstrip amplifier circuits for optimization of the diode size to ensure a reasonable gain per stage with minimum dc power dissipation.

Unpackaged diodes with integral plated heat sinks were mounted on small gold-plated copper blocks [5.08 x 5.08 x 2.54 mm (0.2 x 0.2 x 0.1 inch)] for attachment to the microstrip circuit. This diode mounting scheme, in addition to minimizing the interconnect parasitics, produces a low thermal resistance while providing flexibility in diode replacement. Appropriate lengths of bond wire were used to provide the necessary lumped inductance to resonate with the effective diode capacitance and achieve the desired center frequency of operation. A frequency-scaled version of the X-band dc block⁷ was used as the dc block. This dc block has a coupling length of 2.29 mm (0.090 inch), a spacing-to-height (s/h) ratio of 0.1, and a width-to-height (w/h) ratio of 0.2 for patterns etched on alumina substrates ($\epsilon = 9.5$). The single-stage circuit consists of two quarter-wave transformer sections and a dc block etched on 0.25 mm alumina substrates. At first, this circuit was used in conjunction with a commercially available circulator for amplifier optimization. An array of tuning pads was used for fine microwave tuning. Generally, a small-signal gain of 10 to 15 dB can easily be obtained with a 1 dB bandwidth in excess of 500 MHz. The optimum diameter for Ku-band IMPATT diodes with a breakdown voltage in the range of 38 to 42 V was determined to

be $\sim 0.90 \mu\text{m}$ (3.5 mils) with a corresponding capacitance at zero bias of 1 pF. This amplifier stage generally dissipates ~ 0.5 to 0.7 W of dc power (14 to 18 mA, 41 to 43 V) and will form the basis for the integration of the three-stage preamplifier.

The Ku-band MIC circulators described in Section III.B.1 were incorporated in the multistage amplifier design shown in Figure 18. The circulator-isolator chains and the coupling networks were fabricated on single-ferrite and alumina substrates, respectively. Each substrate had a dimension of $4.3 \text{ cm} \times 1.02 \text{ cm}$ (1.692 inch \times 0.4 inch) and was mounted on a gold-plated aluminum housing with a silver-based conductive epoxy. A 0.25 mm (10 mil) step in the ground plane was provided to accommodate the difference in the thickness of the ferrite [0.5 mm (20 mils)] and alumina [0.25 mm (10 mils)] substrates. The transitions between the two circuits on the two substrates were connected with gold straps using a split tip welder. A section of a 50Ω line with a gradual bend was included as part of the interconnecting arms between the cascaded circulators. The spacing between two circulators is 9.25 mm (0.364 inch). The optimum spacing has been determined by the design tradeoff between maintaining a compact size and ensuring maximum isolation between adjacent stages. One stage of isolation is used between the second and third amplifier stages. A piece of lossy material placed on the isolation port increases the isolation ($> 25 \text{ dB}$) between the output and input over a wide frequency range ($> 1 \text{ GHz}$). A cover with ECCOSORB coating (not shown in the figure) was used for this amplifier. The lossy material eliminates spurious radiations and/or "box" resonances. The dimensions of the advanced integrated amplifier are $5.08 \times 3.05 \times 1.5 \text{ cm}$ (2.0 \times 1.2 \times 0.6 inch). Figure 19 shows the microwave performance characteristics of the preamplifier, with rf input level as a parameter. From this figure it is seen that at the design input level of -20 dBm , more than 35 dB gain can be obtained within the amplifier band (13.4 to 13.650 GHz). With reduced rf input the gain increases, and a substantial increase in the amplifier ripple occurs. This distortion in



47-1867



TEXAS INSTRUMENTS
INCORPORATED

Figure 18 Photograph of the Advanced Integrated Preamplifier

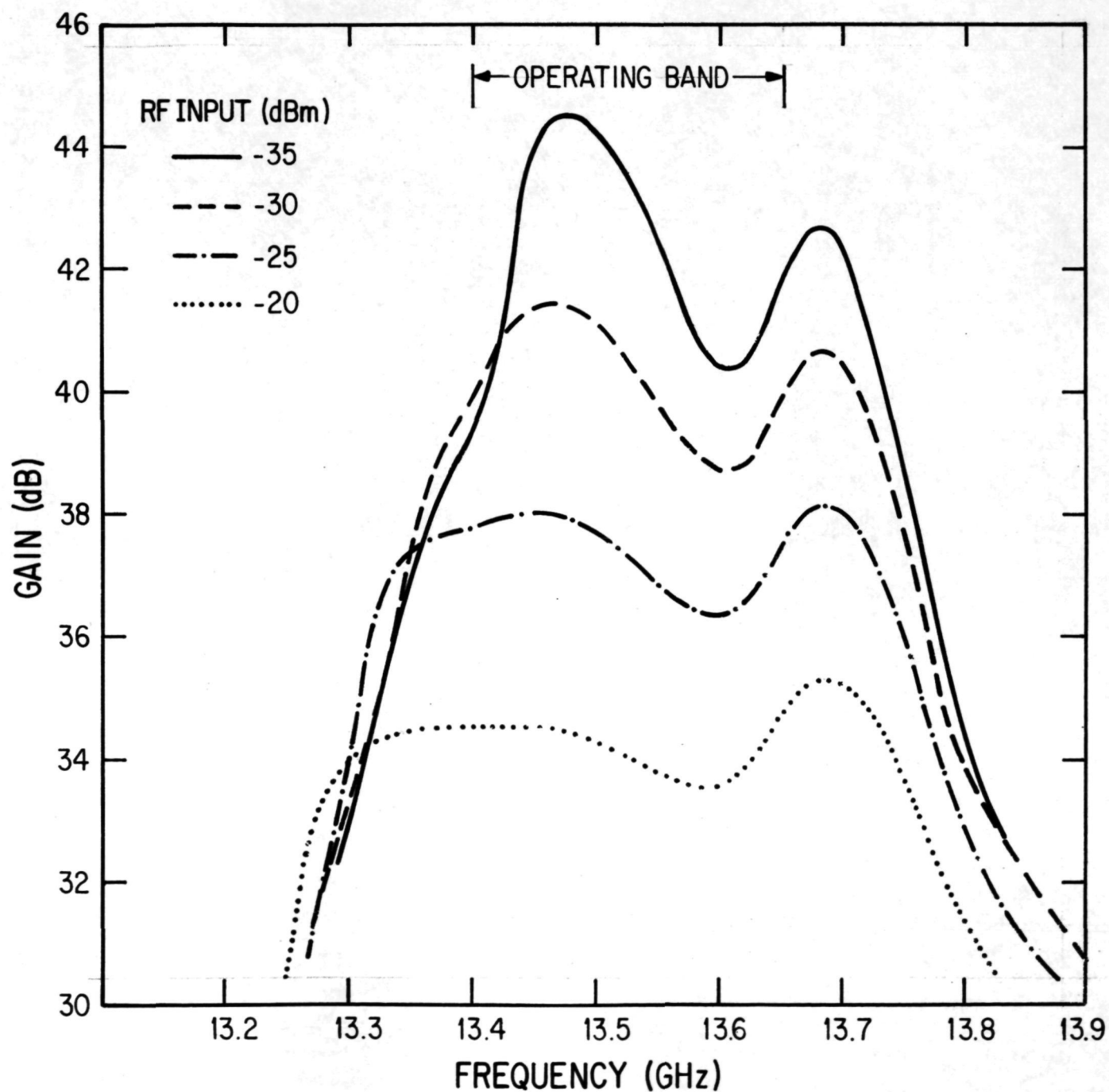


Figure 19 Performance Characteristics of the Preamplifier Shown in Figure 18

response is due to the rf level dependence of the active impedance of the diode. It will have a minimum effect on the overall ripple of the transmitter, since this ripple will be reduced even at low drive levels by the power amplifier that will be operated in saturation. Nevertheless, stagger-tuning can be employed to minimize the bandpass ripple for the preamplifier if required. A single, common bias voltage of 42 V was applied to all three stages of the amplifier. The unit dissipates 2.5 W (60 mA at 42 V) with no external cooling required.

Third-order intermodulation measurements were performed on the preamplifier. Two tunable Gunn oscillators in waveguide cavities were used as the signal sources. The output spectrum was observed with an HP8555A spectrum analyzer. Figures 20 and 21 show the fundamental signal output and the third-order intermodulation product versus the input level at the lower band edge frequency and band center, respectively. In all cases, two cw input signals of the same amplitude and with 10 MHz separation were applied to the amplifier. From these figures it is seen that the measured third-order intermodulation product of this amplifier is more than 20 dB below the fundamental signal output level with two -33 dBm cw input signals applied.

Variation of the gain-frequency response with ambient temperature has also been characterized for the preamplifier. Figure 22 shows the measured amplifier temperature performance. Compensation of the gain response was achieved over the temperature range from 19°C to 65°C by increasing the amplifier current from 62 mA at 19°C to 65 mA at 65°C. The gain was maintained at 35 dB across the amplifier band (13.4 to 13.65 GHz) with less than 1 dB variation. The main effect of increasing the junction temperature is to increase the capacitive susceptance of the diode and, thus, lower the frequency for maximum gain of a series-resonated diode.

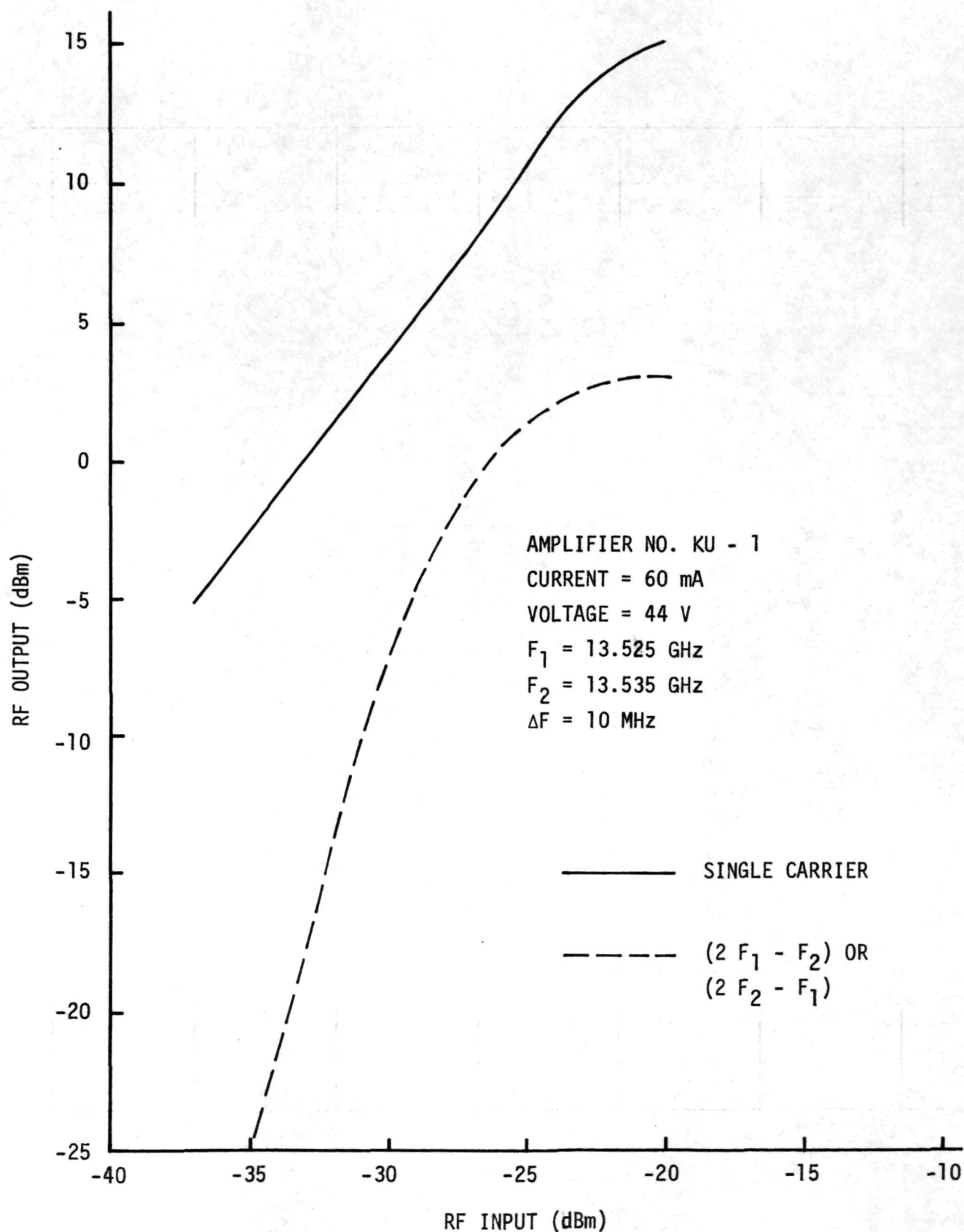


Figure 20 Third-Order Intermodulation Product vs Input Level at Lower Band Edge of the Preamplifier

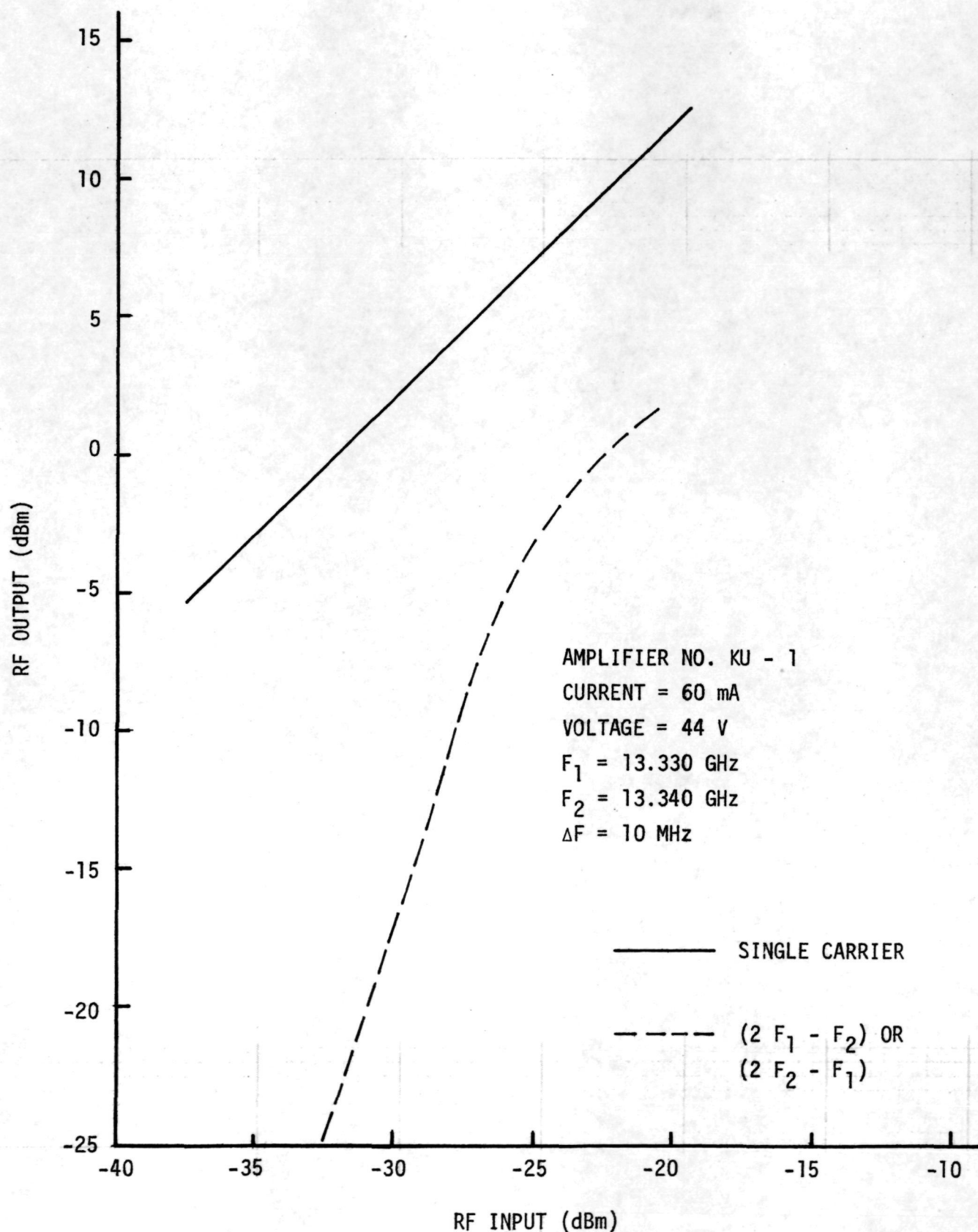


Figure 21 Third-Order Intermodulation Product vs Input Level
at Band Center of the Preamplifier

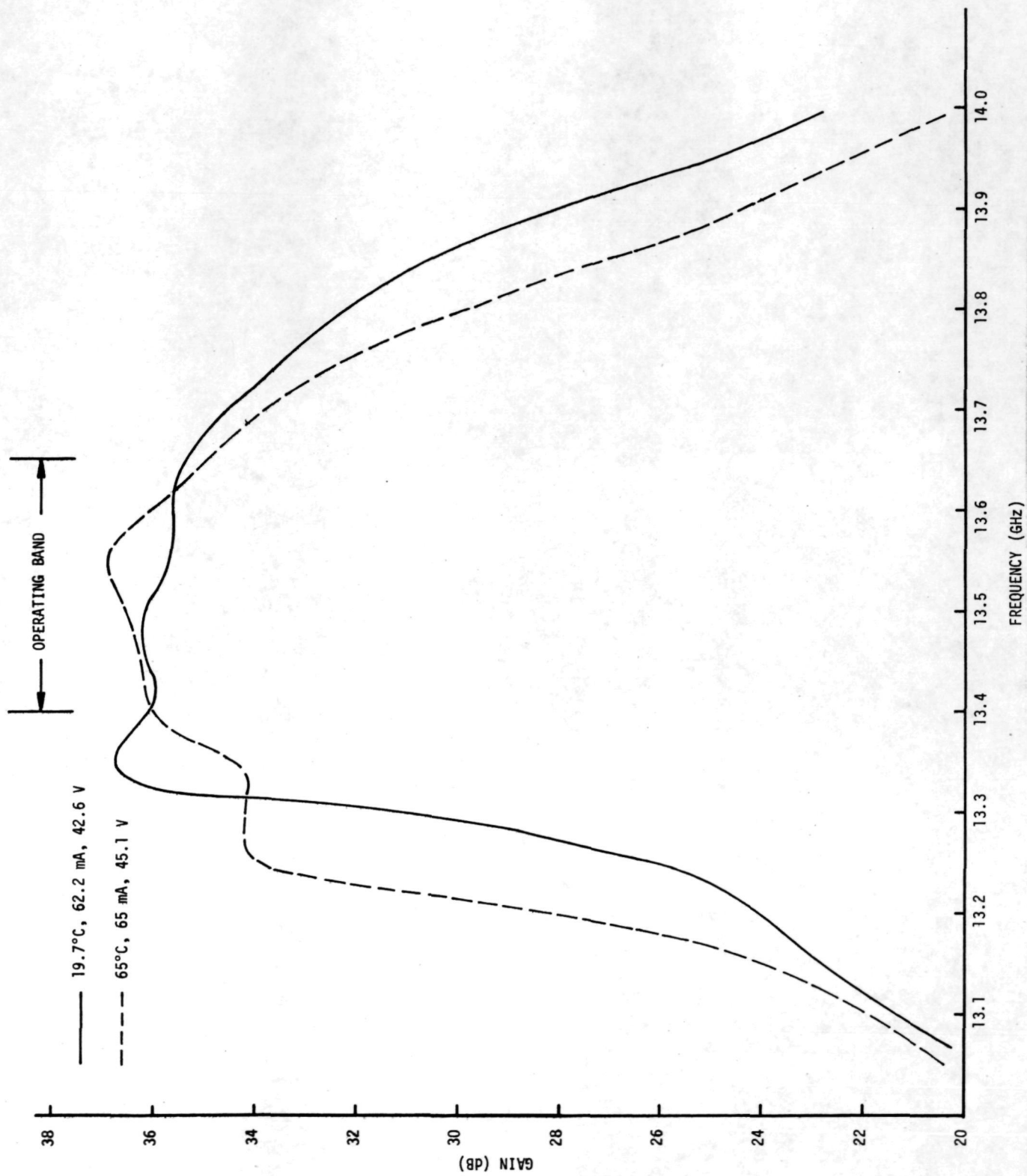


Figure 22 Temperature Performance of the Preamplifier

3. Power Amplifier Design and Performance

Cascading of several Read diode amplifier stages will be required to fulfill the performance goals of the power amplifier section of the spacecraft transmitter. The power amplifier is to be designed with an output power of 5 W at a gain of ~ 21 to 22 dB across the 13.4 to 13.65 GHz frequency band. Microwave characterization of these diodes is essential for determining a successful amplifier design when the high-power, high-efficiency capabilities of the Read diodes are to be fully utilized.

Diodes from different material growth and process runs were evaluated in coaxial package form in a Ku-band waveguide oscillator circuit, determined to be suitable for further study, and mounted on microstrip diode carriers (the gold-plated copper block described earlier) for electrical characterization. The characterization process included both microstrip oscillator evaluation and single-stage microstrip amplifier measurements.

The primary reason for operating the diodes in an oscillator circuit was to study the large-signal impedance characteristics. Once the oscillator circuit is tuned for large-signal operation, the large-signal diode impedance can be inferred from a measurement of the circuit impedance with a network analyzer. Of particular importance is the measurement of the subharmonic impedance of the circuit, since proper subharmonic loading is critical in preventing parametric oscillations and premature power saturation. To prevent this undesirable effect, the circuit must present a relatively high value of admittance, preferably inductive at these frequencies. Any high Q resonances near the subharmonic frequency would be detrimental to large-signal operation and should be avoided.

The most direct approach for large-signal device characterization is to use a single-stage microstrip circuit tuned for amplification. A variety of amplifier circuit topologies have been used to characterize the Read diodes.

Gain compression, susceptibility to parametric oscillations, and tuning flexibility are the three most important factors in the design of the matching network. The results of the study outlined above and the characterization of diodes from several slices indicated that a circuit of the same type used for the preamplifier stages provides the best compromise between device performance and circuit stability for Read diodes. A circuit design of this type was selected for the power amplifier stages.

Figure 23 shows the gain-frequency response of a single-stage Schottky-Read amplifier. At the highest input level of + 27 dBm, the amplifier is capable of 2 W cw output power with 6 dB gain and 22.4% power-added efficiency. The 1 dB bandwidth is 1 GHz (13 to 14 GHz).

Figure 24 shows the rf performance of the same amplifier versus the input power. The gain drops from 17 dB at small signal levels to 6 dB at the highest input power shown. At intermediate drive levels the gain is almost constant because of the automatic dc current increase with increasing input levels due to the rectification effects. Figure 25 shows the bias characteristic of the amplifier. The bias voltage drops from 44 V under small-signal conditions to 38 V under large-signal operation, with a corresponding increase of current from 120 mA to 170 mA, as determined by the bias load line. The amount of voltage dropback varies from slice to slice, but it is generally on the order of 7 to 10 V, depending on the small-signal bias point and the bias load line. Because of these large-signal rectification effects, a bias load line with some finite resistance must be provided. The optimum value of this resistance is determined by the desired "quiescent" operating point and the requirement for minimum power dissipation. The significance of the bias characteristics on the design of the dc-to-dc converter is discussed later in this report.

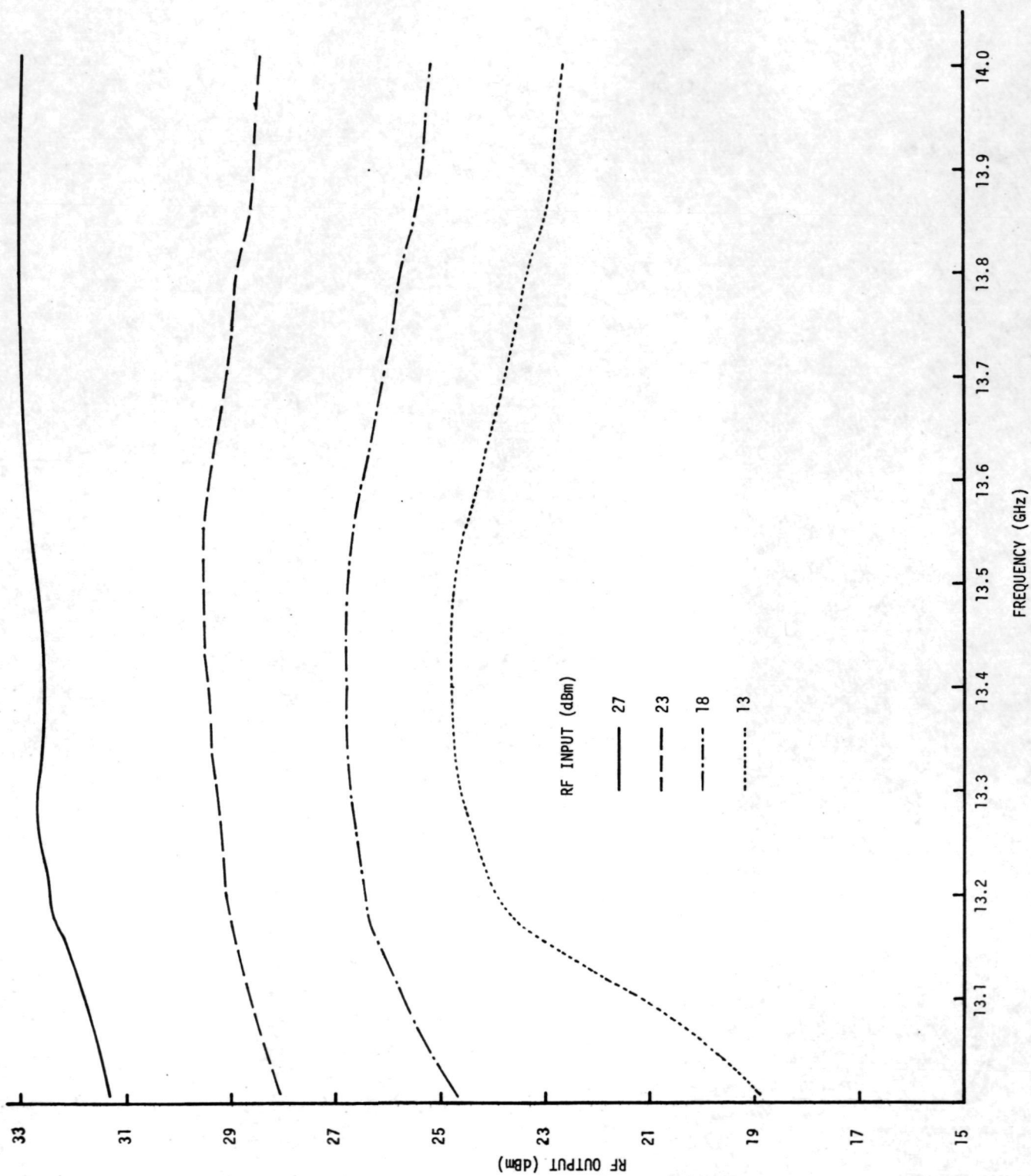


Figure 23 Gain-Frequency Response of a Single-Stage Schottky-Read Microstrip Amplifier

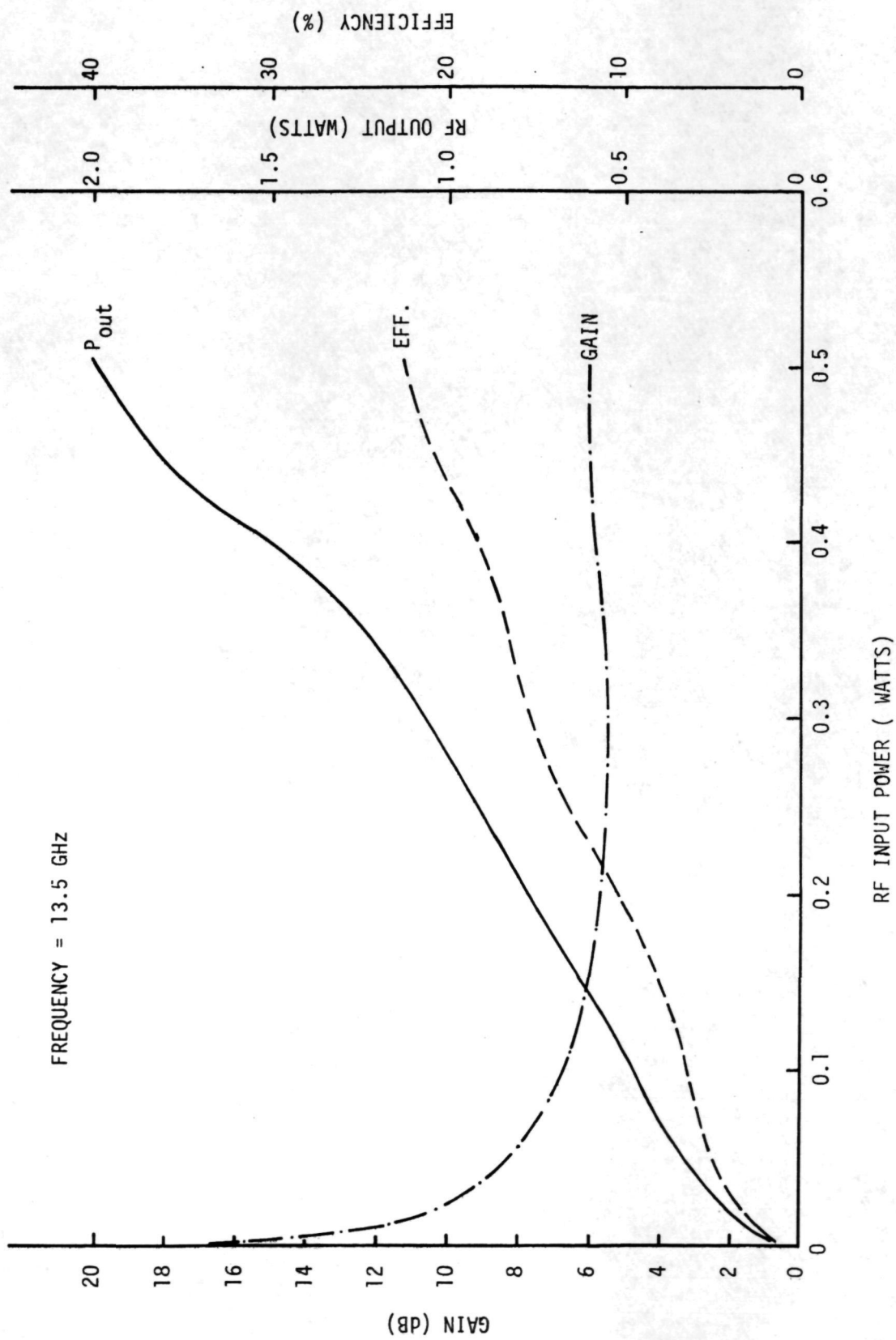


Figure 24 RF Performance of a Single-Stage Schottky-Read Amplifier

FREQUENCY = 13.5 GHz
BIAS LOAD LINE = 100 OHMS

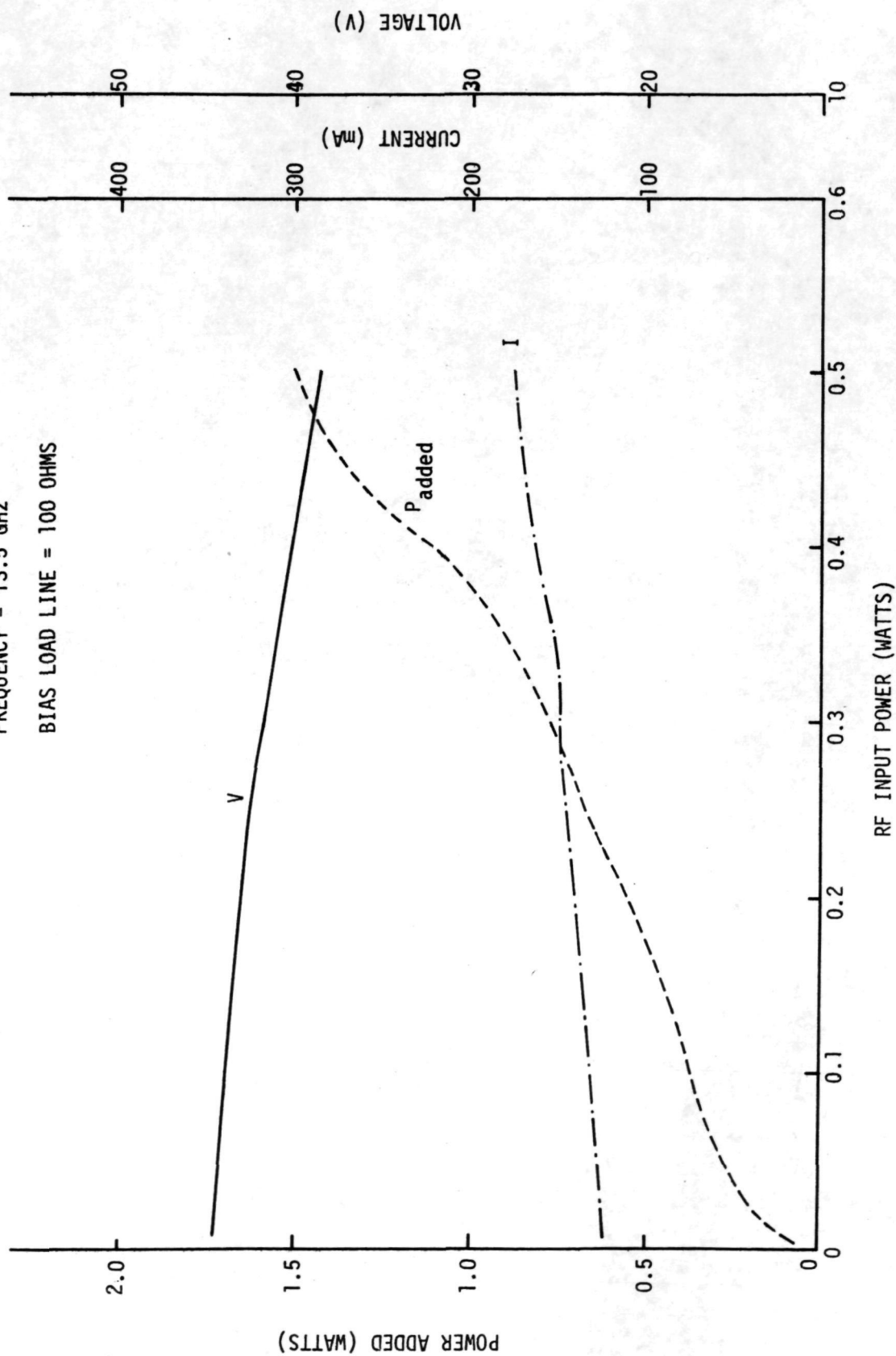


Figure 25 Bias Characteristics of a Single-Stage Schottky-Read Amplifier

To achieve the 5 W output power goal, a double-mesa diode capable of generating at least 4 W of microwave power must be used for the last stage of the power amplifier. The highest output power obtained with a single-stage amplifier was 5.9 W at 4 dB gain and 22% power-added efficiency at a frequency of 13.4 GHz. Figure 26 shows the output power, efficiency, and gain performance of this single-stage amplifier as a function of the rf input levels. A similar amplifier gave higher gains at lower output power levels, with gains of 5.5, 6.2, and 6.5 dB at output powers of 4.17, 3.89, and 3.31 W, respectively. The corresponding power-added efficiencies were 17.9, 18.7, and 18.1%. Double-mesa diodes were used for both amplifiers. The diameter of each mesa was 127 μm (5 mils). The two mesas were connected with a 0.127 mm (5 mil) wide gold strap. The two mesas are separated by about 0.5 mm (20 mils) to achieve a significant reduction of the thermal resistance of the diode compared with an equal-area single-mesa diode. The breakdown voltage of the diode for optimum microwave performance is in the range of 20 to 30 V. The exact value is a function of the high-low doping level combinations and the thickness of the high layer.

Concurrent with the task to achieve the output power goal was an effort to establish bias circuit techniques to eliminate the small-signal oscillation problem associated with the severe gain compression exhibited by Read amplifiers. Several amplifiers were stabilized by reducing the resistive load line presented by the bias circuit. Because of large-signal rectification effects, the bias current increases and the device operating voltage decreases when the input rf signal is increased. Figure 27 shows the gain compression characteristics of a double-mesa Schottky-Read amplifier at two frequencies. It is seen that a higher small-signal gain would result in a higher large-signal gain. Figure 28 shows how the operating I-V characteristics of this amplifier depend on the rf input level for different load lines. The static I-V curve without rf input power is shown for the amplifier tuned for no oscillations. The bias state for maximum efficiency and output power of the

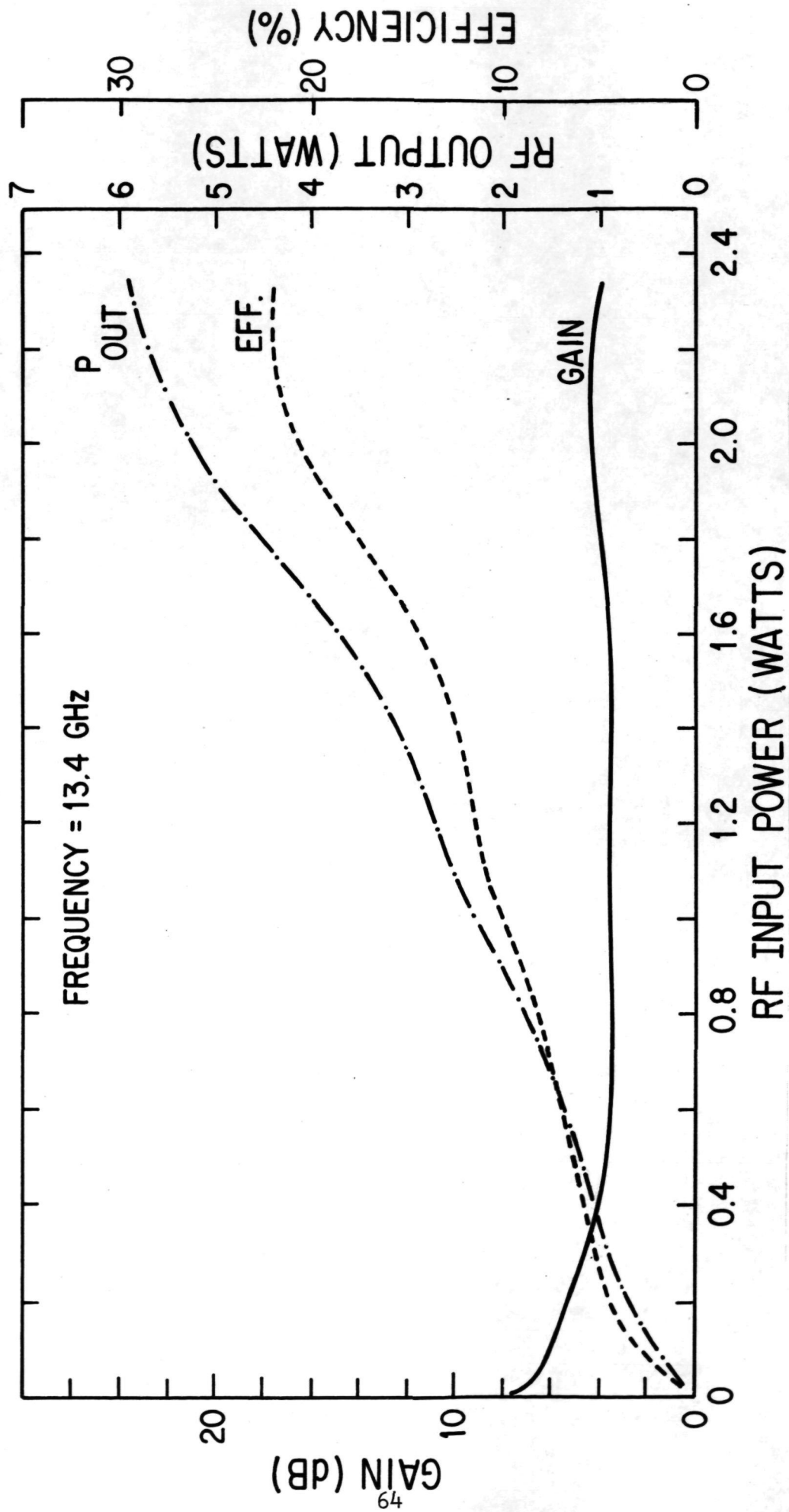


Figure 26 RF Performance of a Double-Mesa, Single-Stage Schottky-Read Amplifier

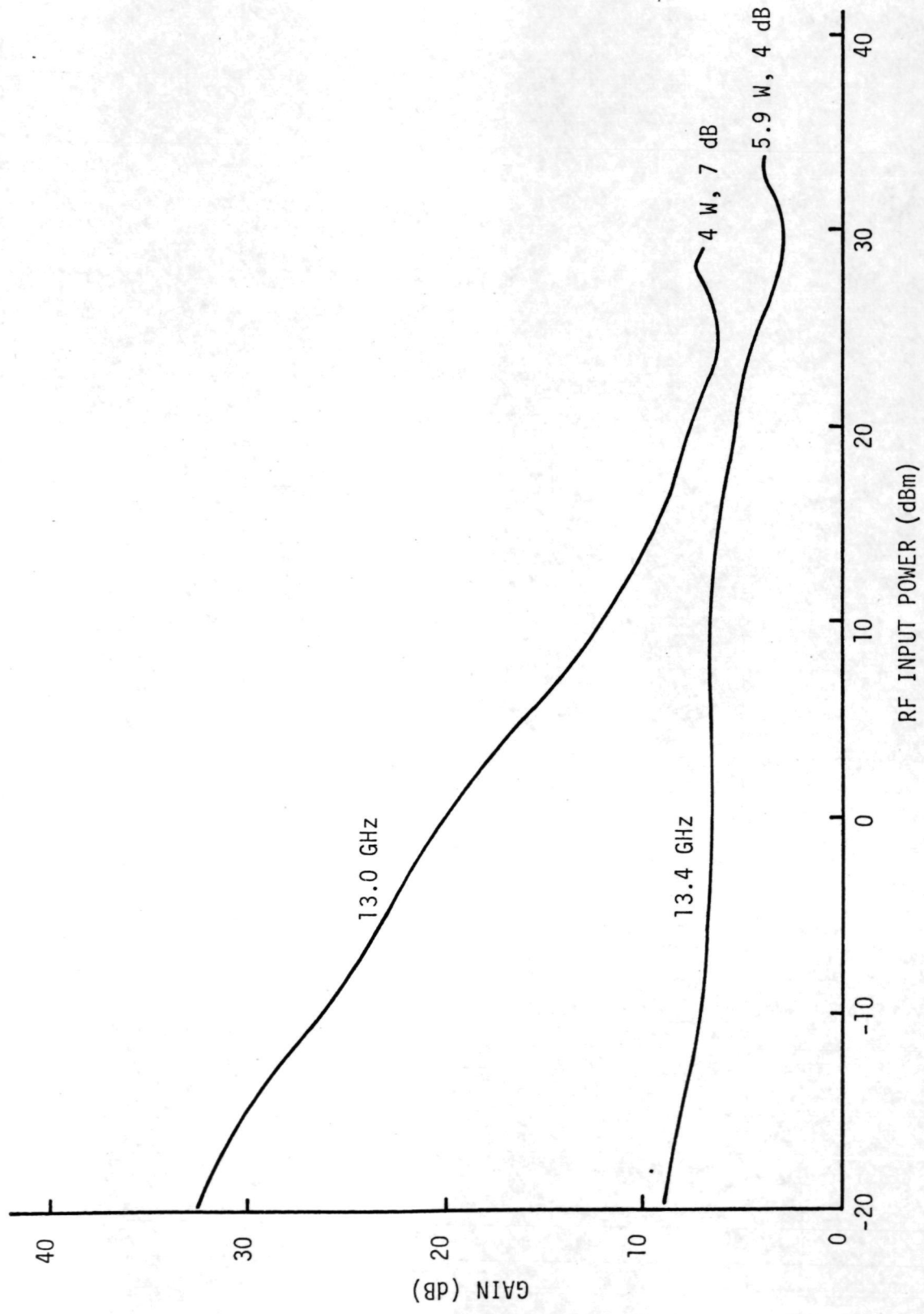


Figure 27 Gain Compression Characteristics of a Double-Mesa Schottky-Read Amplifier at Two Frequencies

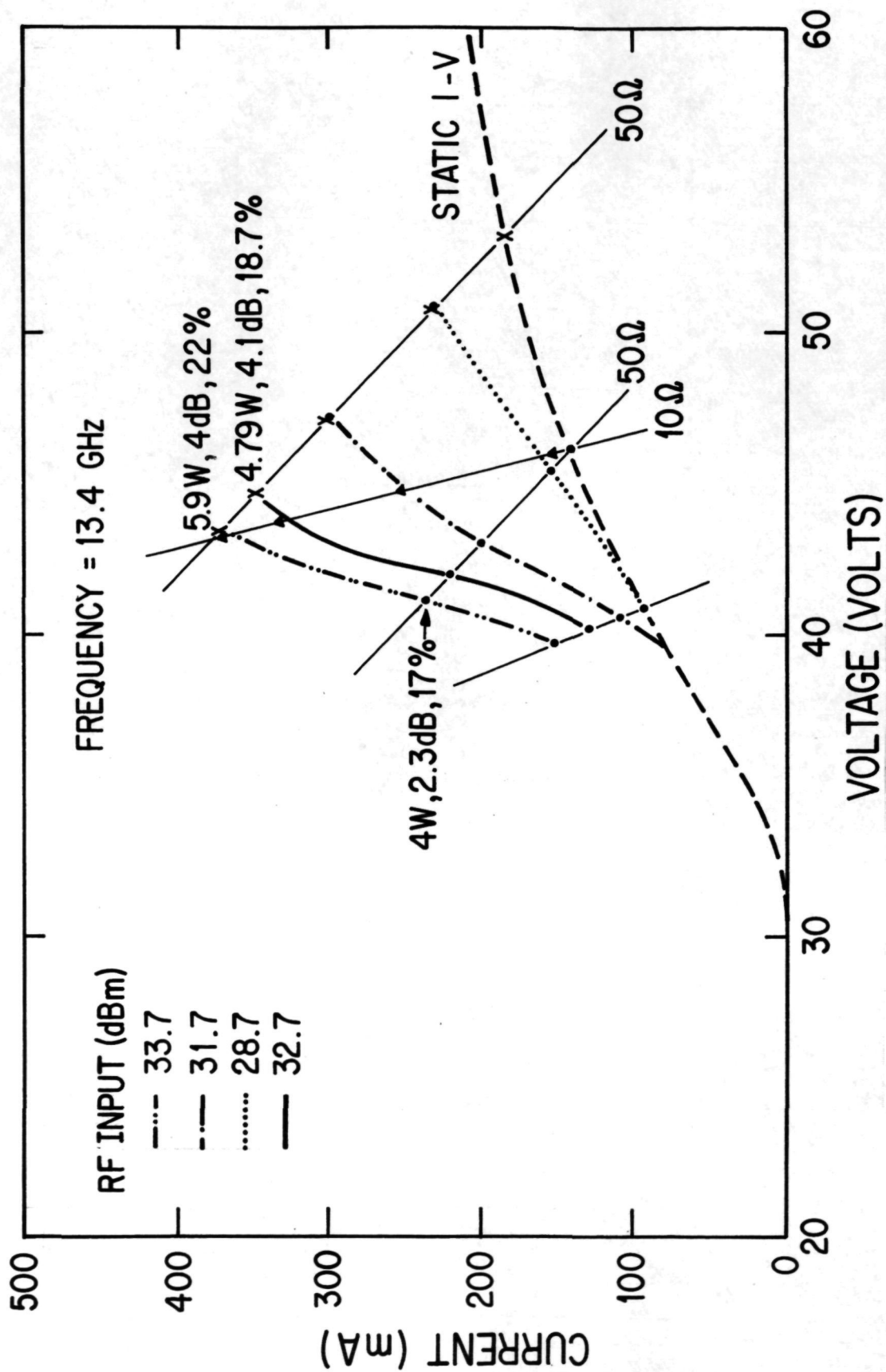


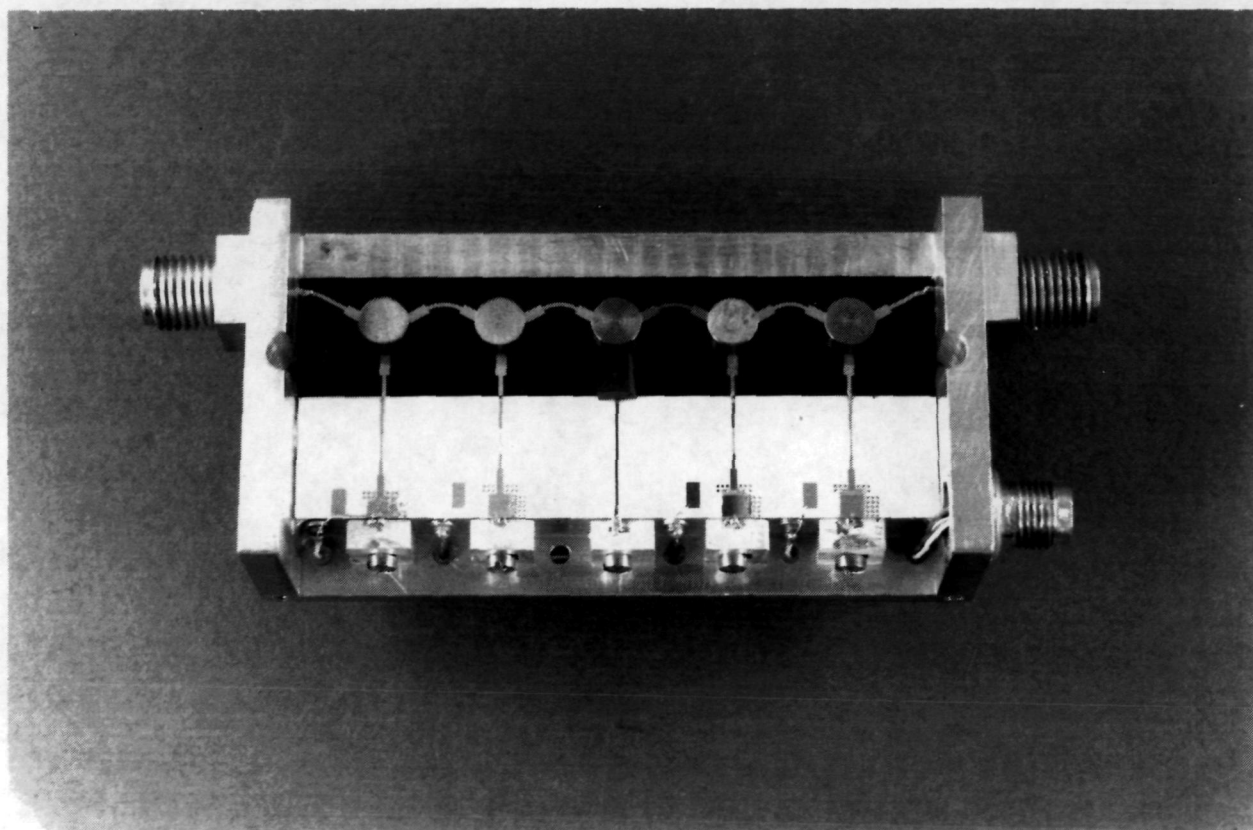
Figure 28 Operating I-V Characteristics of a Schottky-Read Amplifier

amplifier can be reached by a careful selection of the bias circuit load line. Use of a low value of bias resistance to reach the optimum large-signal bias point is desirable because the gain at small signal levels is much lower. While this scheme of using low values of bias resistance is effective in stabilizing a single-stage Read diode amplifier, it is still not completely satisfactory when several stages are cascaded in an amplifier configuration. This is because the high overall small-signal gain can cause spurious oscillations below certain rf drive levels. In addition, the low values of bias resistance required may not be compatible with the requirement to minimize the bias oscillations caused by rf signal induced low-frequency negative resistance.

Due to the severe gain compression exhibited by the Read diodes under large-signal operation in single-stage amplifiers, the original three-stage power amplifier design was modified to include four stages. Figure 29 is a photograph of the integrated four-stage amplifier. Relatively few problems were encountered in the design of the first three stages that incorporate single-mesa diodes. The amplifier dimensions are $5.7 \times 3.05 \times 1.5$ cm ($2.25 \times 1.20 \times 0.60$ inch).

Figure 30 shows the gain versus frequency response of a four-stage power amplifier. An output power of 4 W with 20 dB gain was achieved with this amplifier. The amplifier is centered at a frequency of 13.5 GHz with a 1 dB bandwidth of 1.1 GHz. The overall power-added efficiency is 15%.

Figure 31 shows the microwave performance curves of another four-stage power amplifier at two input power levels. At an rf input of + 15 dBm, an output power of 36.5 dBm (4.5 W) was obtained with 21.5 dB gain. When the rf input power was lowered to 5 dBm, 36 dBm (4 W) of output power was obtained at 31 dB gain.



1875-167



TEXAS INSTRUMENTS
INCORPORATED

Figure 29 Photograph of a Four-Stage Power Amplifier

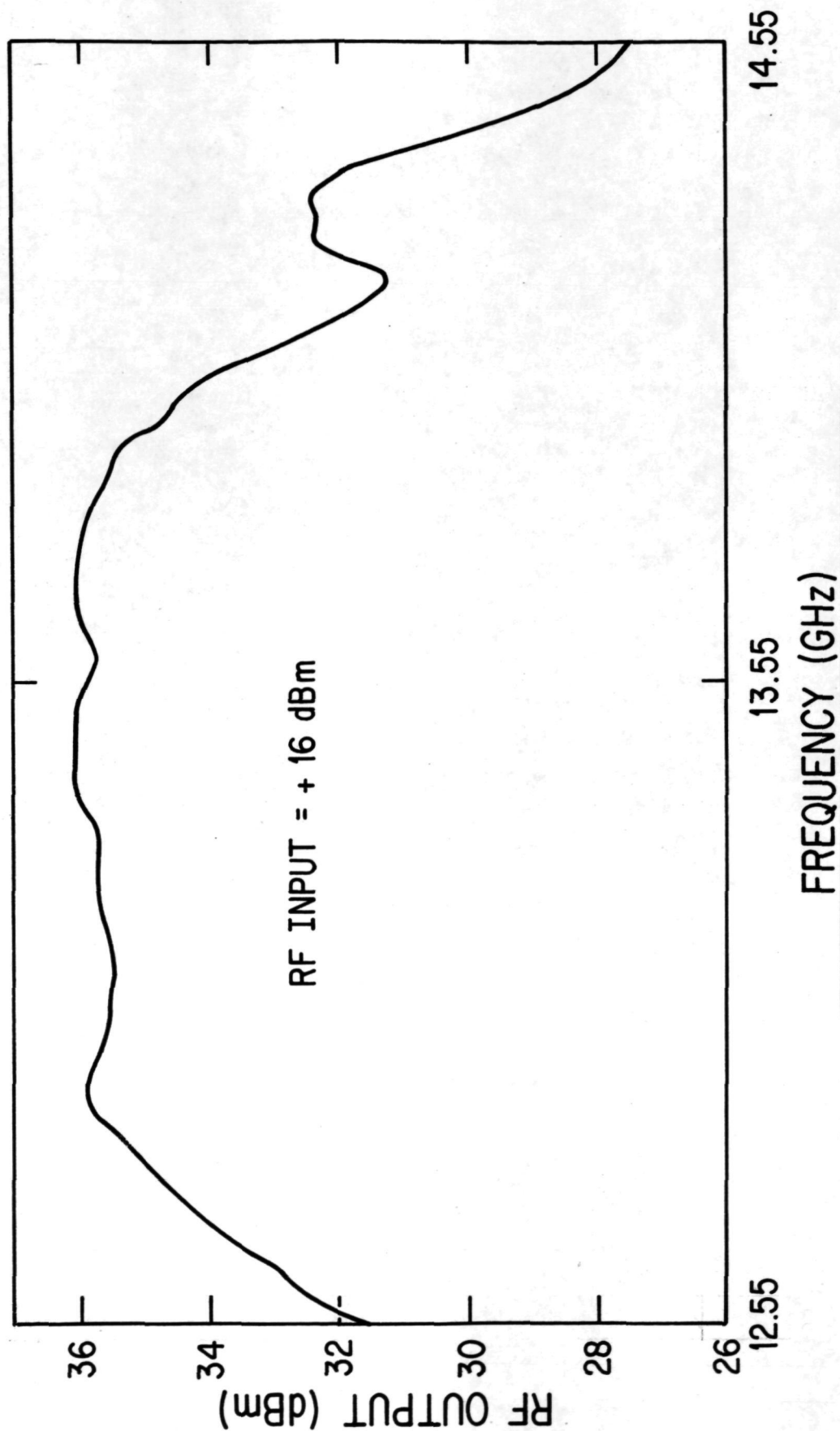


Figure 30 Gain-Frequency Response of a Four-Stage Power Amplifier

OPERATING
BAND

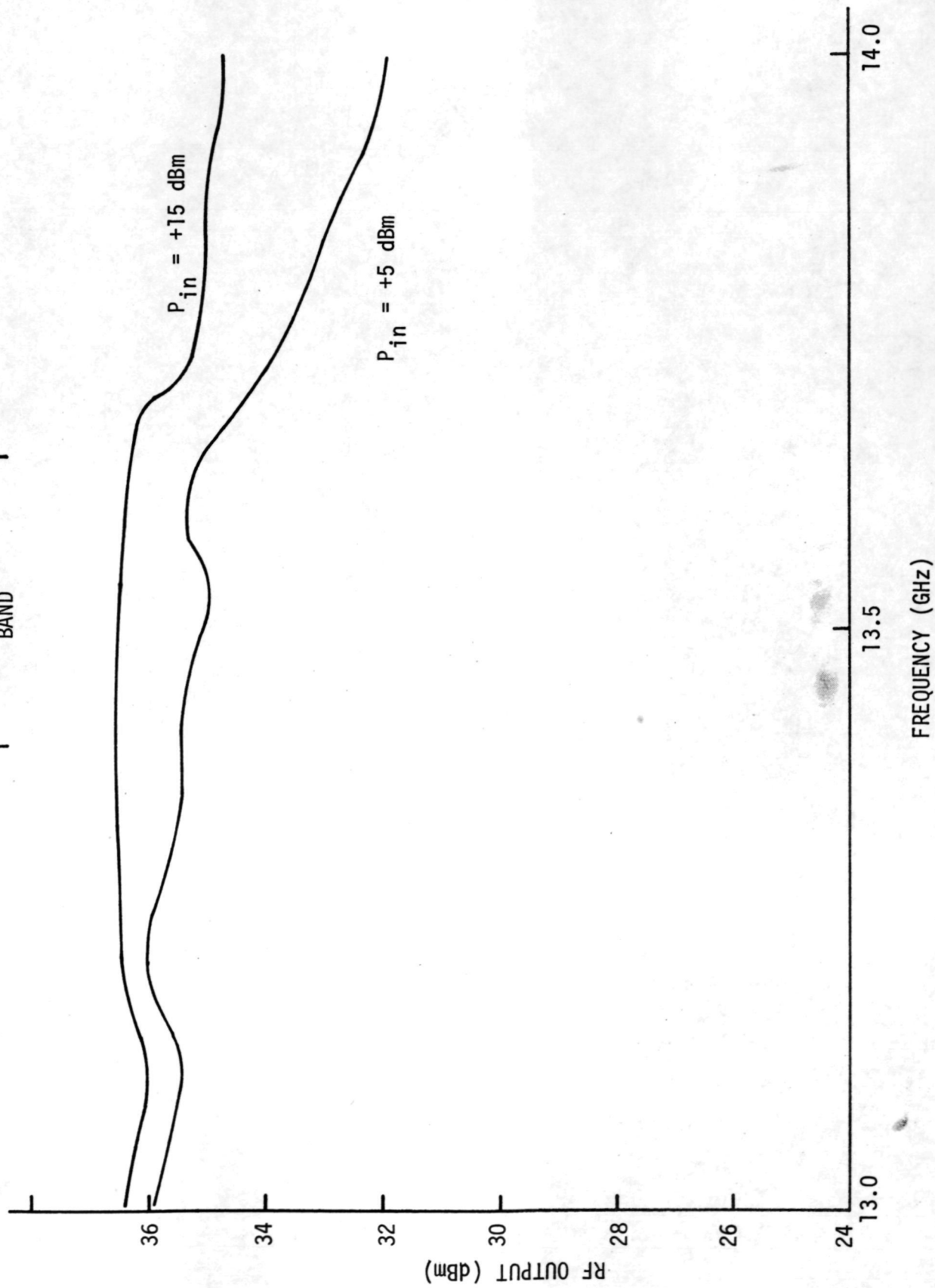


Figure 31 Gain-Frequency Response of the Second Four-Stage Power Amplifier

Although the above amplifiers generally provide stable amplification with rf input levels in the range of 0 to 16 dBm, a spurious signal is present when the input signal is reduced below 0 dBm. This spurious signal is a result of free oscillation caused by high small-signal gain of the Read diode amplifier.

4. Dc Power Supply Design

- Dc-to-Dc Converter

A schematic diagram of the dc-to-dc converter is shown in Figure 32. The converter is of the switching type and uses a saturable transformer to step up the voltage, which is then filtered to provide the dc output. This converter accepts an input voltage of 28 ± 1 V and supplies an output voltage of 59 ± 2 V.

- Voltage Regulator

To minimize the effect of supply voltage fluctuations on amplifier performance, a constant voltage regulator was incorporated in the output of the converter. Figure 33 is a schematic diagram of the regulator. The output voltage changes less than 120 mV for a 2 V input change to the converter. At an input of 28 V and 1.79 A (50 W) to the dc-to-dc converter, a regulated output voltage of 54 V is obtained at 74% overall efficiency.

- Bias Networks

The use of high values of bias resistance would be desirable from the point of view of minimizing bias line oscillations, if it were not for the desire to reduce the tendency for oscillation at low input levels. As discussed earlier, the selection of low bias resistance allows the amplifier to be biased at lower current under small signal condition. This is especially true for the high-power output stages.

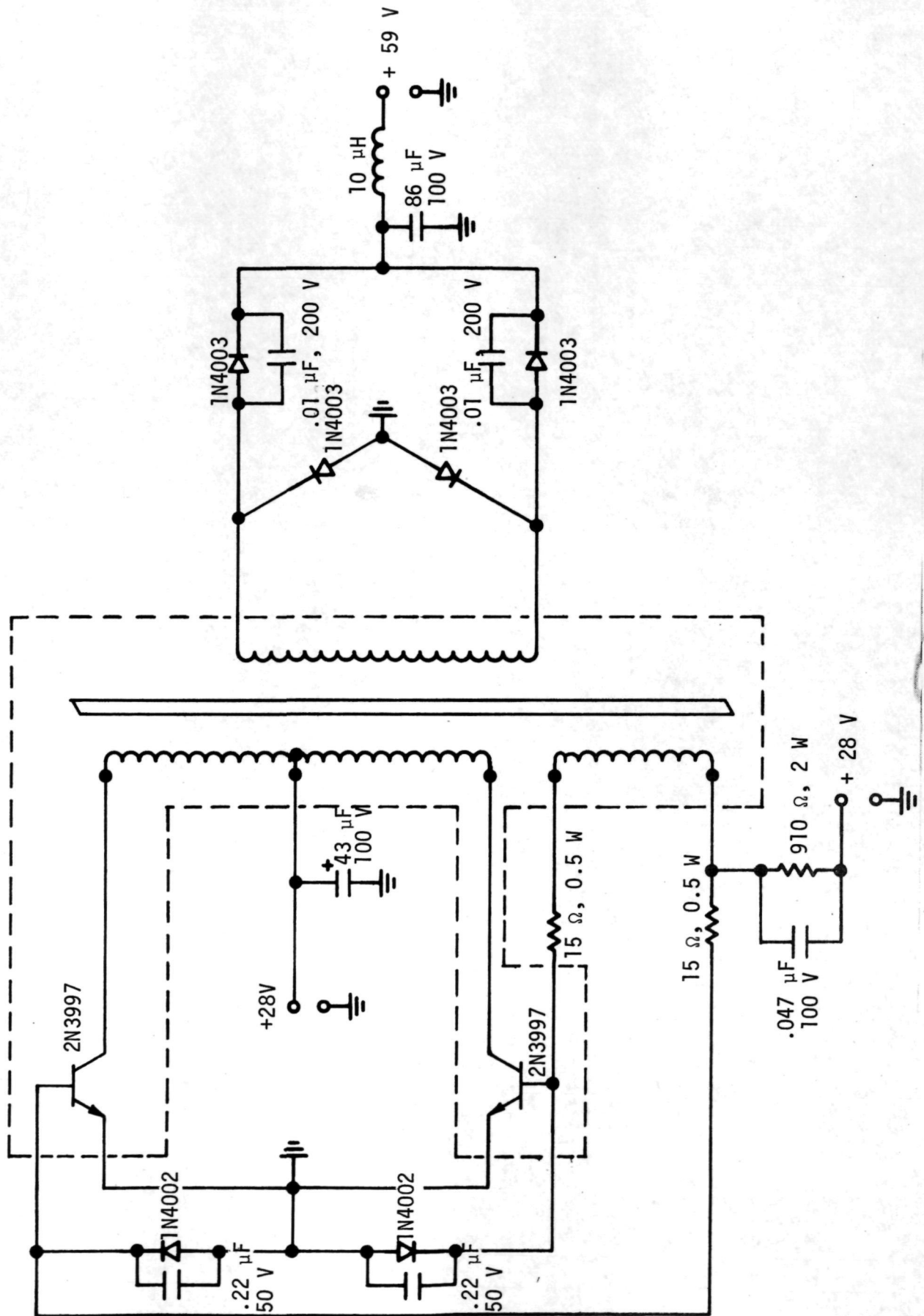


Figure 32 Schematic Diagram of the dc-to-dc Converter

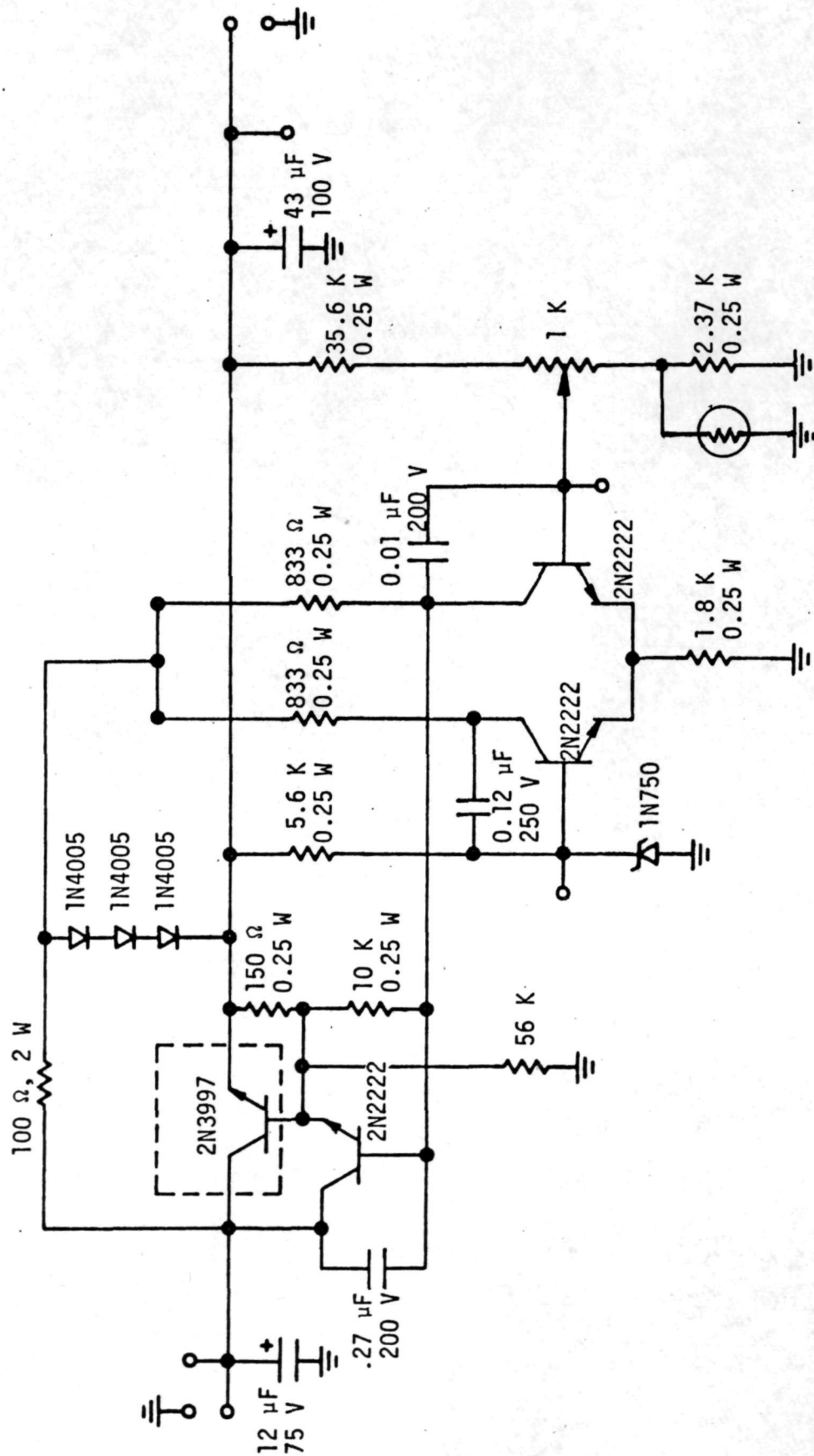


Figure 33 Schematic Diagram of the Voltage Regulator

Figure 34 shows the bias networks used for the breadboard transmitter module to be described later. Except for the last two stages, a simple bias resistor is used for each of the amplifier stages. In the last two stages, a zener diode with appropriate breakdown voltage was used to set the voltage drop across the collector and base of the power transistor when the transistor is turned on. An appropriate value of load resistance can then be connected between the emitter and the diode to provide the desired load line.

5. Breadboard Transmitter Module

As a first step toward the final integration of the breadboard transmitter module, the preamplifier and the power amplifiers were cascaded in an effort to achieve the desired gain and output power. Because of the extremely high gain of the cascaded amplifier, a discrete isolator with more than 20 dB of isolation was used between the two amplifiers for additional input/output isolation. Figure 35 shows a block diagram of the transmitter configuration. The design output powers and gain budgets of each stage are shown in the figure.

Figure 36 shows the gain-frequency response of a cascaded amplifier. Within the operating band of the amplifier, 3 W of output power with 55 dB gain was obtained. A single-mesa Read diode was used for the last stage of the power amplifier in this case. Figure 37 shows the microwave performance of another amplifier. At the highest input level of -20 dBm, this amplifier provided 4.5 W of output power with 56.5 dB gain. A gain of 65.5 dB was obtained with 3.5 W output when the input level was dropped to -30 dBm. Both of these cascaded amplifiers were powered with individual power supplies for each of the seven amplifier stages to optimize the overall amplifier performance, especially with regard to gain-frequency response and minimum spurious oscillations. An appropriate bias resistor was used in series with each of the constant voltage power supplies. The dc voltage and current values were recorded for each stage with and without rf input signals. As has been noted, because of the large-signal rectification effects, the dc current and voltage

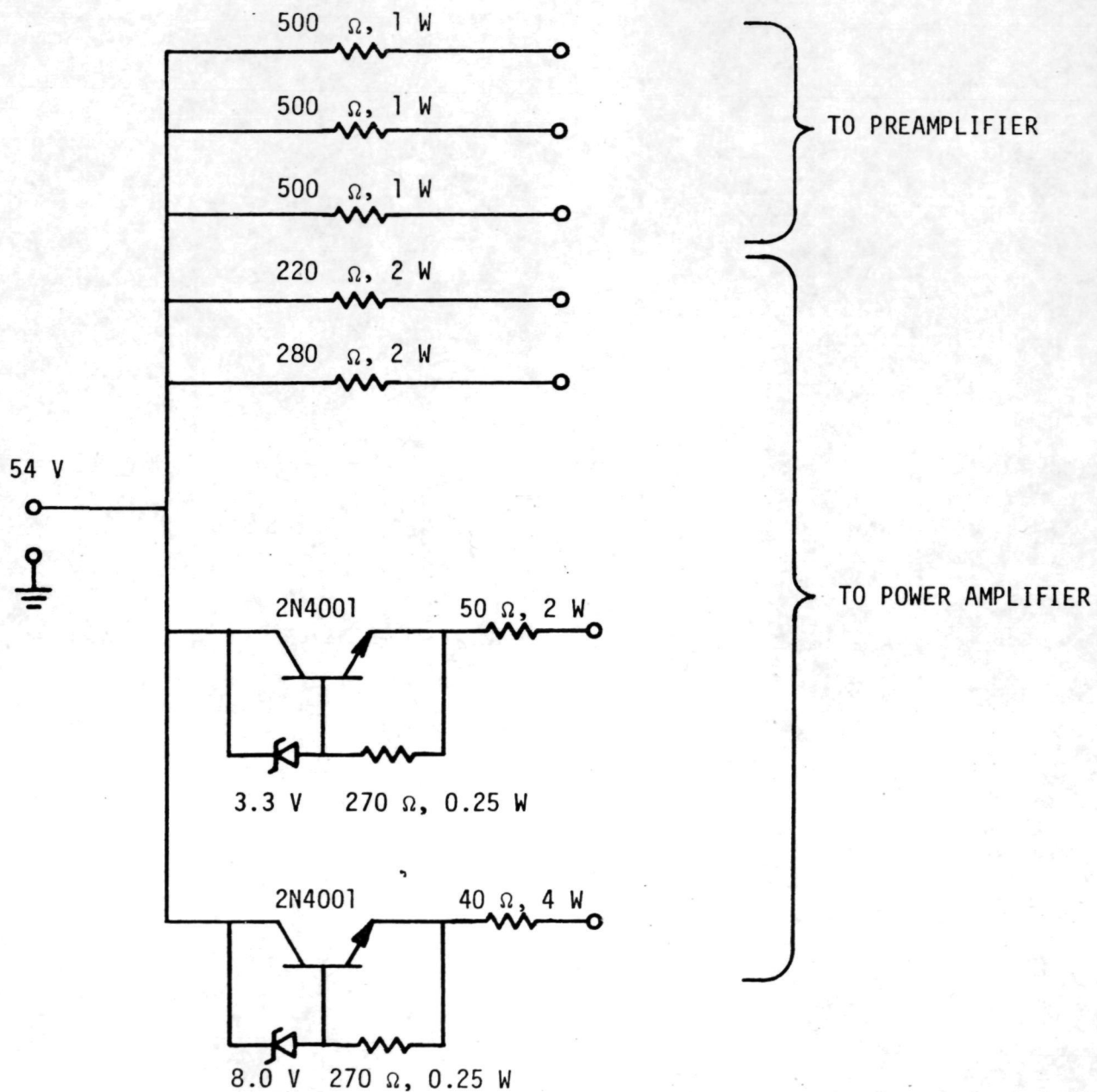


Figure 34 Bias Networks for the Cascaded Amplifier

STAGE	I	II	III	IV	V	VI
Gain (dB)	13.0	13.0	10.3	8.3	7.0	6.0
DC Input (Watts)	.5	.5	.5	1.39	5.6	16.72
RF Output (Watts)	0.0002	0.004	0.04	0.269	1.26	5.0
RF Power Added (Watts)	0.0002	0.004	0.039	0.251	1.12	4.18
Efficiency (%)	0.04	0.8	7.8	18.0	20.0	25.0

*0.3 dB Loss between two circulator junctions

*RF power shown in dBm

*Overall module efficiency = 10%

*Efficiency of DC to DC converter = 67.2%

*Overall amplifier efficiency = 19.8%

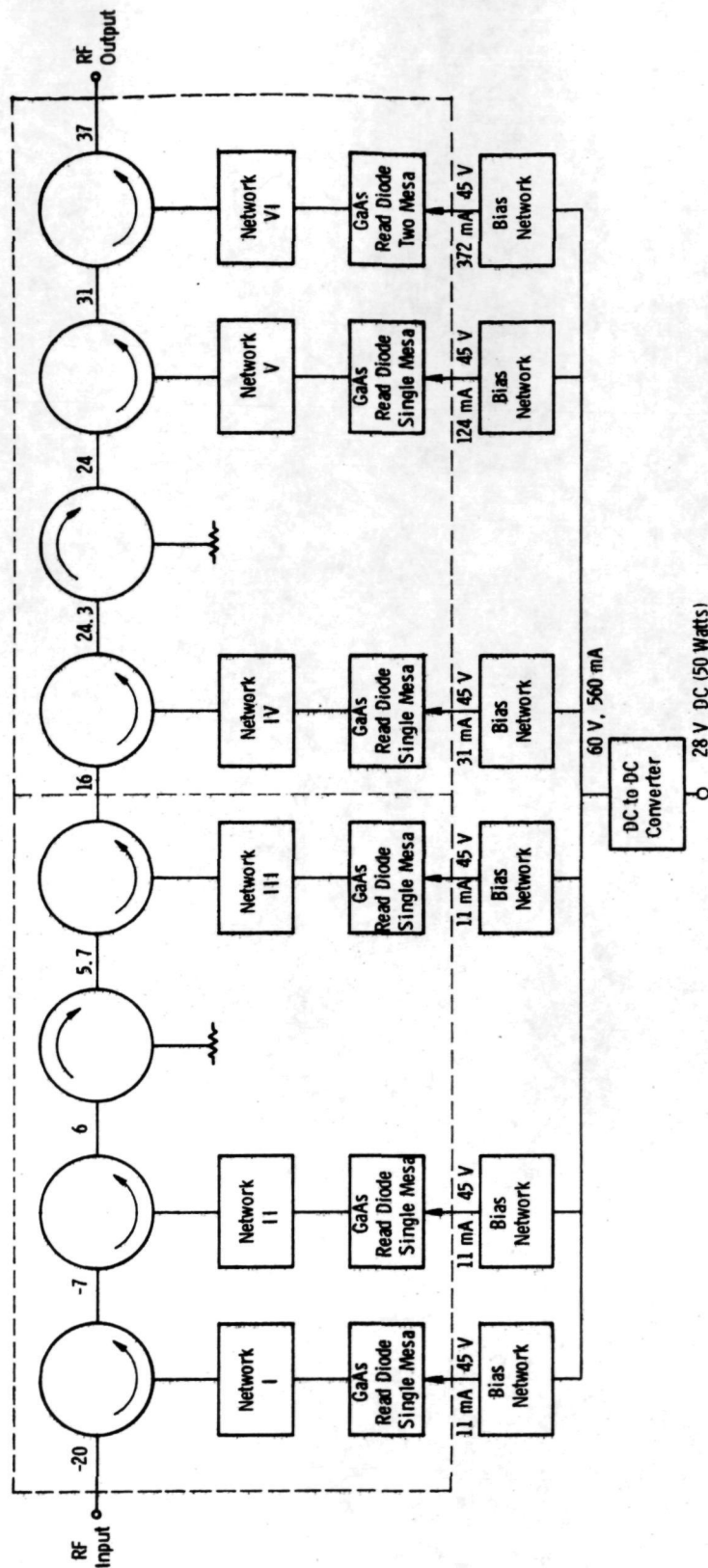


Figure 35 Block Diagram of Transmitter Configuration

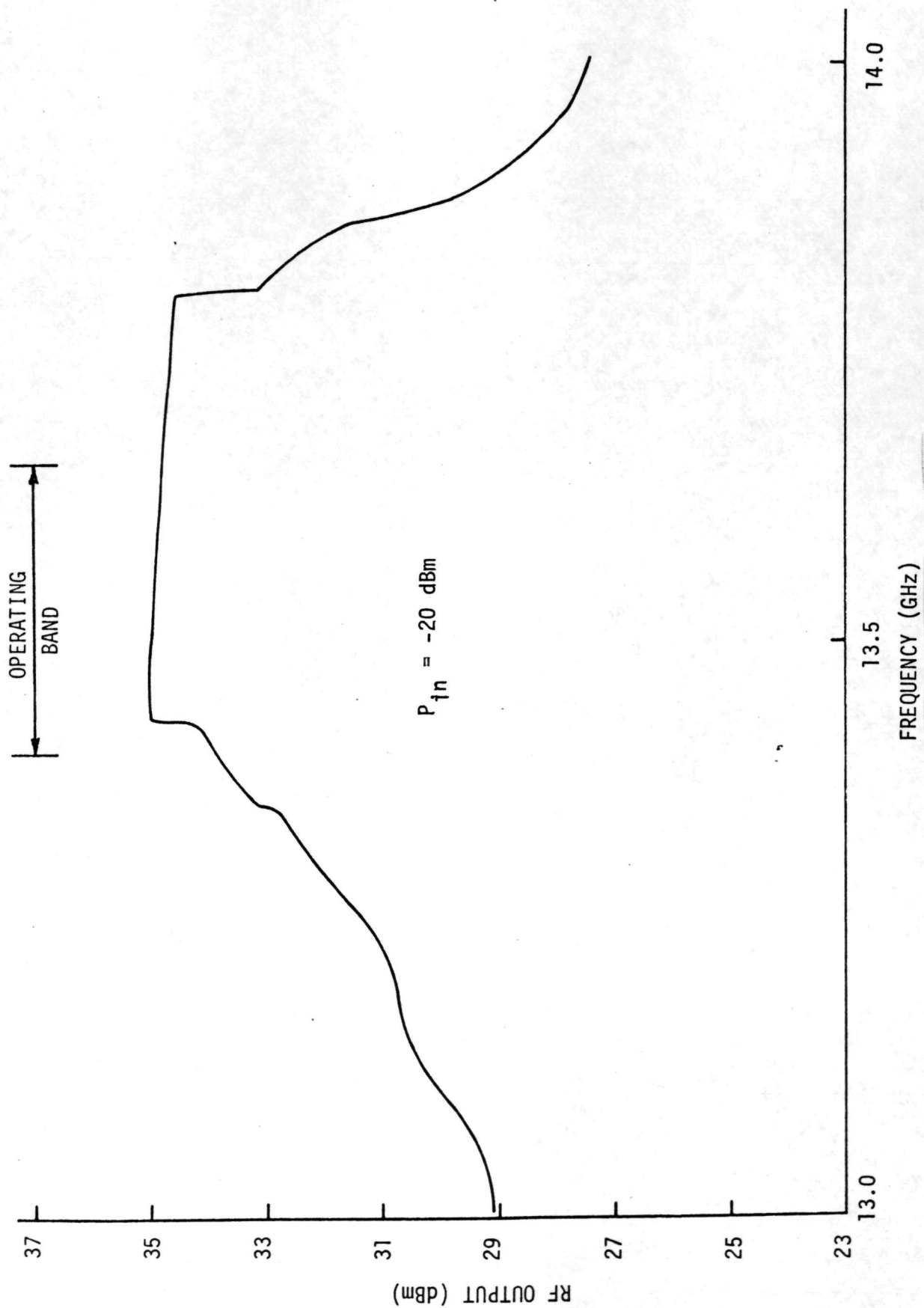


Figure 36 Microwave Performance of the Cascaded Amplifier I

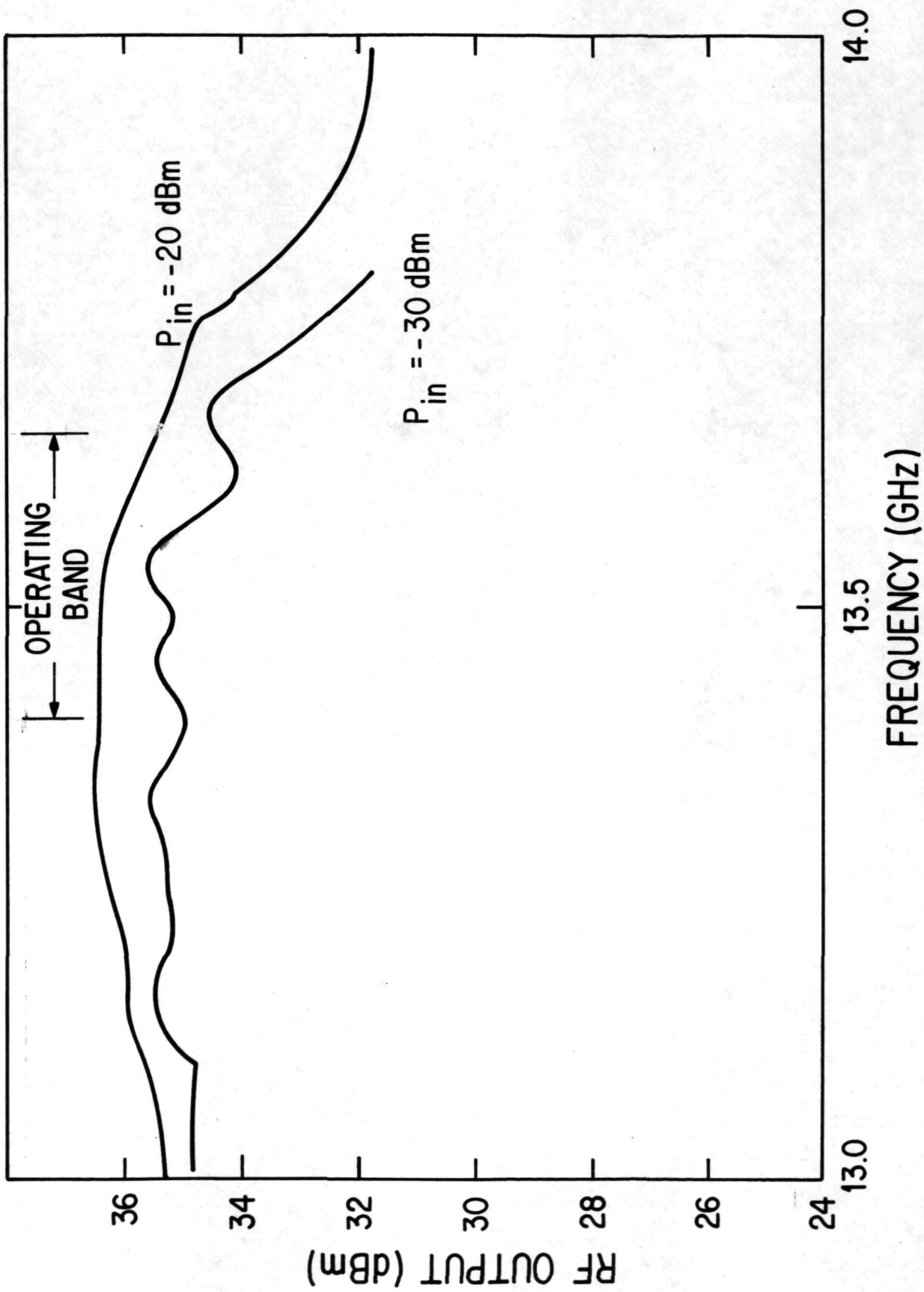


Figure 37 Microwave Performance of the Cascaded Amplifier II

under operating conditions are quite different from those values obtained with no input signal, especially for the high-power Read diode stages. Obtaining these bias point values is important for the design of the bias network to be discussed later.

Figures 38 and 39 show the housing of the breadboard module and its associated components. The housing is made of aluminum and has outer dimensions of $7.0 \times 3.6 \times 2.4$ inches (991 cm^3), which is within the maximum allowable volume of 1000 cm^3 . The housing is divided into two compartments, one for the preamplifier and power amplifier modules and the other for the dc-to-dc converter, the voltage regulator, and the bias networks. The amplifier compartment is further divided into two decks, the upper deck for the preamplifier and the lower deck for the power amplifier. A discrete isolator has been used to increase the isolation between the two amplifiers. The complete module weighs approximately 1.13 kg (2.5 pounds).

The operations of two different preamplifier-amplifier combinations were described earlier in this section. One cascade combination delivered 3 W using a single-mesa Read diode in the final output stage, while the other delivered 4.5 W with a double-mesa output stage diode. The 3 W amplifier combination was used in the breadboard module delivered at the completion of Phase I. The 4.5 W combination was not available at the time the design requirements for the dc-to-dc converter were firmed up, and there was insufficient time available to make the required changes and still meet the breadboard delivery schedule.

Prior to its final integration into the transmitter module, the bias network, as shown in Figure 34, was used for the preamplifier and power amplifier to determine the optimum load resistance for the individual stage. The supply voltage was set at 54 V. The gain compression characteristics were then measured at different frequencies within the amplifier frequency band. For the

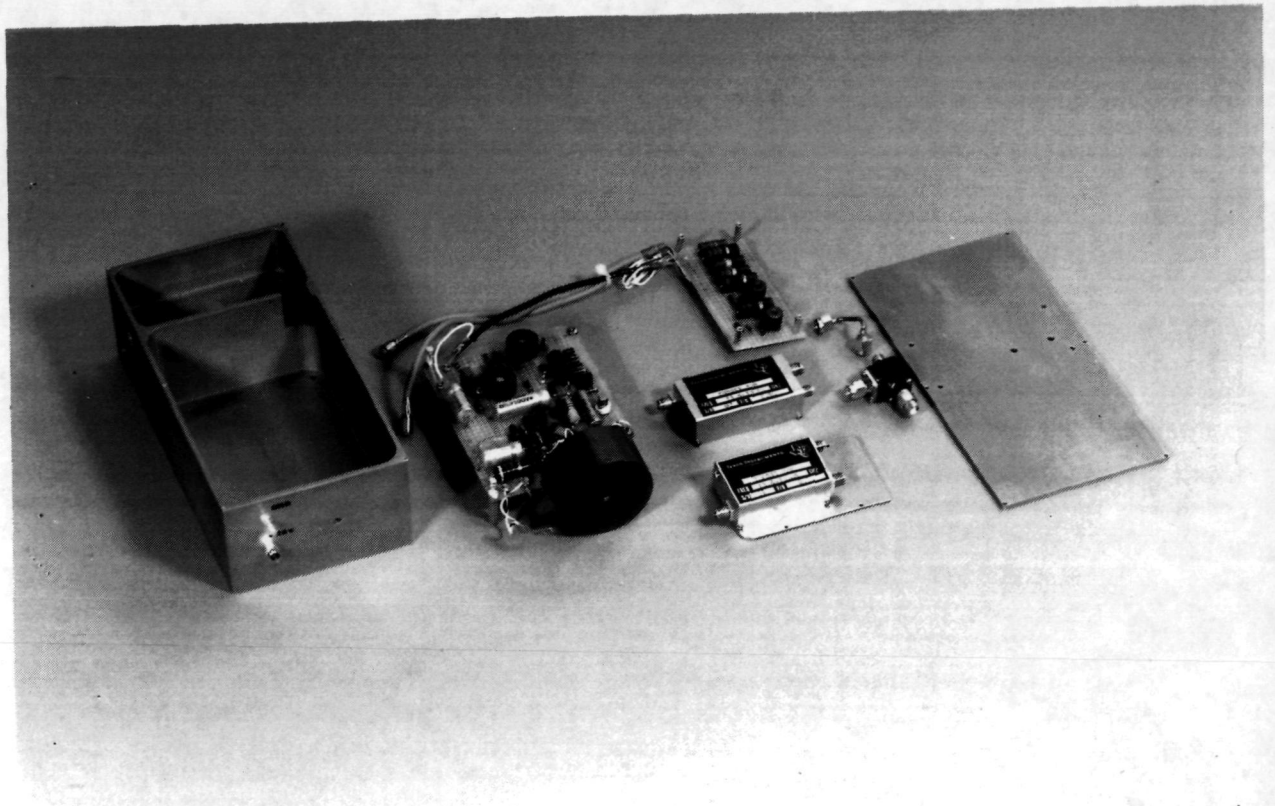


Figure 38 Photograph of the Breadboard Transmitter Module
Showing the Individual Components

*half-tone
included*

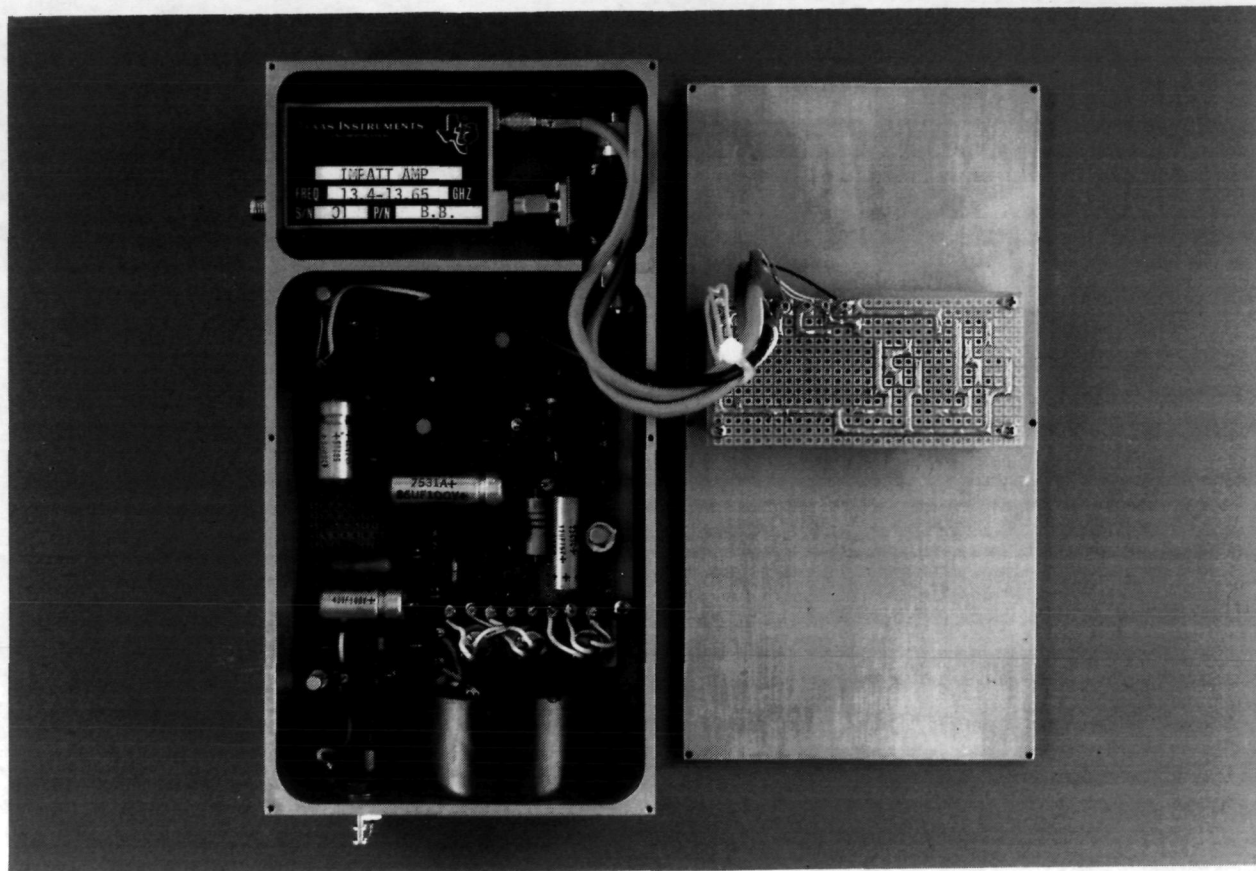


Figure 39 Photograph of the Complete Breadboard Transmitter Module

power amplifier, a small-signal gain of more than 40 dB was measured. At the highest input power of 14 dBm, the gain was 21 dB, which is close to the value obtained when individual power supplies were used. In the absence of the input signal, a spurious signal generally exists. However, this spurious signal disappears when the rf signal is increased above a certain threshold value (-19 to -12 dBm) input for the power amplifier.

The next step in the module integration process is to cascade the preamplifier with the power amplifier, using the bias networks shown in Figure 34. Figure 40 shows the gain compression characteristics of the cascaded amplifier powered with a single power supply of 54 V at two different frequencies. More than 60 dB gain can be obtained for the lowest input power (-30 dBm) shown. The current increases from 430 mA to 550 mA for the rf input signal range shown in the figure.

The final breadboard module integration was achieved by connecting the bias network to the output of the voltage regulator. The output voltage of the regulator was adjusted to 54 V for a 28 V input to the dc-to-dc converter. At the amplifier center frequency (13.525 GHz), an output power of 3 W was obtained with 55 dB gain. The module dissipates 45 W of input power (28 V and 1.6 A). For rf input signals below -20 dBm, the output is susceptible to spurious output oscillations caused by a high small-signal gain of the amplifier.

Intermodulation measurements have been attempted on the power amplifier and the complete module. At + 14 dBm input power, the third-order intermodulation product of the power amplifier is 10 to 11 dB below the fundamental signal output level with two cw signals of equal amplitude, 10 MHz apart, applied. However, the intermodulation product degrades to 7 to 8 dB below the fundamental signal for two -30 dBm input to the preamplifier and power in cascade. The reason for this degradation in the intermodulation product due to cascading has been found to be due to the use of a preamplifier with

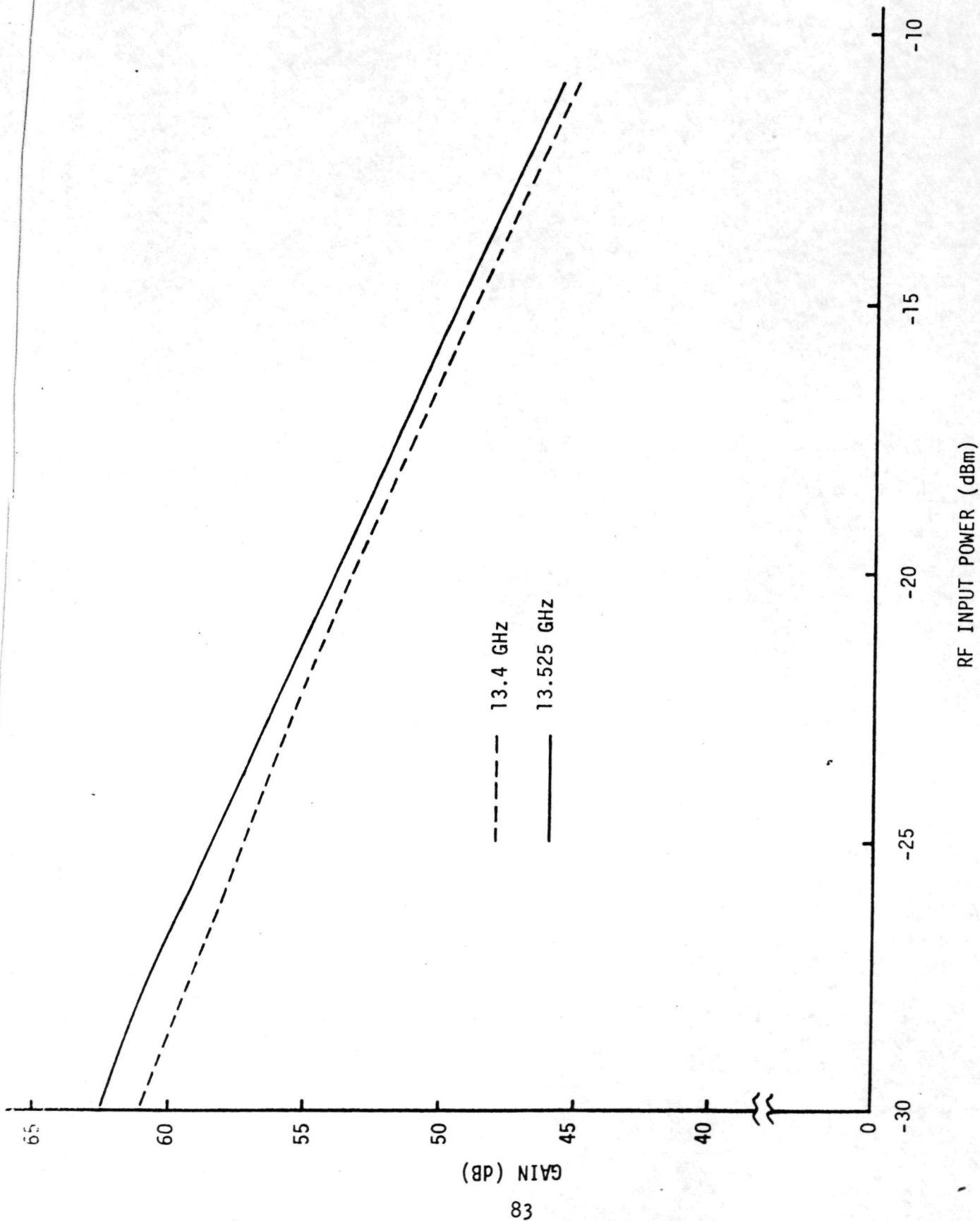


Figure 40 Gain Compression Characteristics of the Breadboard Module

abnormally high intermodulation distortion at a normal output power level. Independent measurements of another preamplifier - power amplifier combination showed that a third-order intermodulation level of -10 to -11 dB can generally be achieved at output power saturation.

Some data were obtained on the temperature performance of the module prior to delivery. The gain of the module was measured at housing temperatures of 20 and 35°C. A decrease of 2 dB in gain was measured with the module supply voltage kept constant at 28 V. The dc current drops from 1.6 A at 20°C to 1.3 A at 35°C for this case. This reduction of gain is expected, since no compensation scheme was used in the breadboard module to adjust the operating voltage at different operating temperatures. As reported previously, the gain of the preamplifier is particularly sensitive to these temperature changes.

The design and performance of the transmitter module were discussed in a paper presented at the 1976 International Solid-State Circuits Conference.⁸

C. Critical Design Problems

Phase I of this contract was completed with delivery of the breadboard spacecraft transmitter. The transmitter module includes a preamplifier, power amplifier, bias networks, voltage regulator, and dc-to-dc converter.

Phase II called for a design improvement effort and the fabrication and testing of two spacecraft transmitters. Although Phase I was successful in demonstrating the feasibility of most of the transmitter goals, a number of design improvements were required. Insufficient time and funds were available for making the required design improvements in Phase II and also fabricating and testing two spacecraft transmitters. Therefore, a proposal to modify the original contract was submitted for approval at the end of Phase I to redirect the program effort toward finding solutions to the following problems identified during Phase I:

- (1) Low yield of suitable Read diodes
- (2) Spurious oscillations at low drive levels
- (3) High level of intermodulation distortion
- (4) Gain rolloff with increasing ambient temperature.

This proposal was subsequently approved, and the modified Phase II program was carried out for six months, ending with the delivery of an improved breadboard spacecraft transmitter.

D. Phase II Breadboard Transmitter Module Development

The major program effort for Phase II was directed toward finding the solutions to the problems outlined in Section III.C. Technical approaches for attacking these problems are given below.

(1) The diode yield problem was addressed by growing additional epitaxial GaAs slices for diode fabrication. Slices with drift doping levels in the range of $5 \text{ to } 8 \times 10^{15} \text{ cm}^{-3}$ were grown. The high layer thickness was optimized by anodic oxidation to yield diodes at about 14.0 to 14.5 GHz. Diodes of this type have shown the best performance in the microstrip amplifier circuits. However, despite these design changes, there was still a lack of suitable high-power, high-efficiency diodes available at the end of Phase II. This problem was discussed in detail in Section II.C. It has been concluded that a possible solution is to use low-high-low structures and thus minimize the harmful effects of tunneling due to the heavily doped layer for efficient Ku-band operation.

(2) The problem of spurious oscillation at low drive levels is inherent in the operation of Read diode reflection amplifiers. This is due to the drastic change of the diode negative resistance as a function of the input drive level. To circumvent this problem, a Schottky barrier diode detector and an MIC directional coupler can be conveniently located at the output of the preamplifier to detect the incoming rf signal and provide a video signal to the voltage regulator for tailoring the supply voltage to the Read diode

stages as a function of rf input signal and to avoid spurious oscillation when the rf input signal drops below a certain level. Figure 41 shows this method schematically. A microstrip directional coupler-detector-assembly, as shown within the dashed line in Figure 41, was fabricated. The directional coupler is located on the input arm of the isolator to be inserted between the preamplifier and the power amplifier module. In this arrangement, an additional degree of isolation can be achieved between the detector and the power amplifier for discrimination against the signal leaking from the self-oscillating Read stages with no rf inputs.

Figure 42 is a schematic diagram of a power supply squelch circuit that can be used to remove the dc power to the Read diode stages if the output power level from the preamplifier drops a predetermined amount as determined by the reference setting of the voltage comparator. In Figure 42 a comparator and a power transistor switch are used to perform the required function. Both the microstrip directional coupler-detector-isolator assembly and the power supply squelch circuit have been incorporated into the Phase II breadboard transmitter module, described later.

(3) Due to the highly nonlinear property of the Read diodes under large-signal operating conditions, a third-order intermodulation level of -10 to -11 dB is generally observed at output power saturation. No degradation of the intermodulation product due to cascaded preamplifier/power amplifier combinations has been observed when a preamplifier with minimum intermodulation distortion is used.

(4) In an effort to maintain a constant gain when the ambient temperature changes, a thermistor was utilized in the control circuit of the constant voltage regulator to tailor the output voltage as the ambient temperature is changed. A total voltage excursion of 4 to 5 V has been achieved with this scheme for temperature compensation. This temperature compensation scheme was used in the Phase II transmitter module described below.

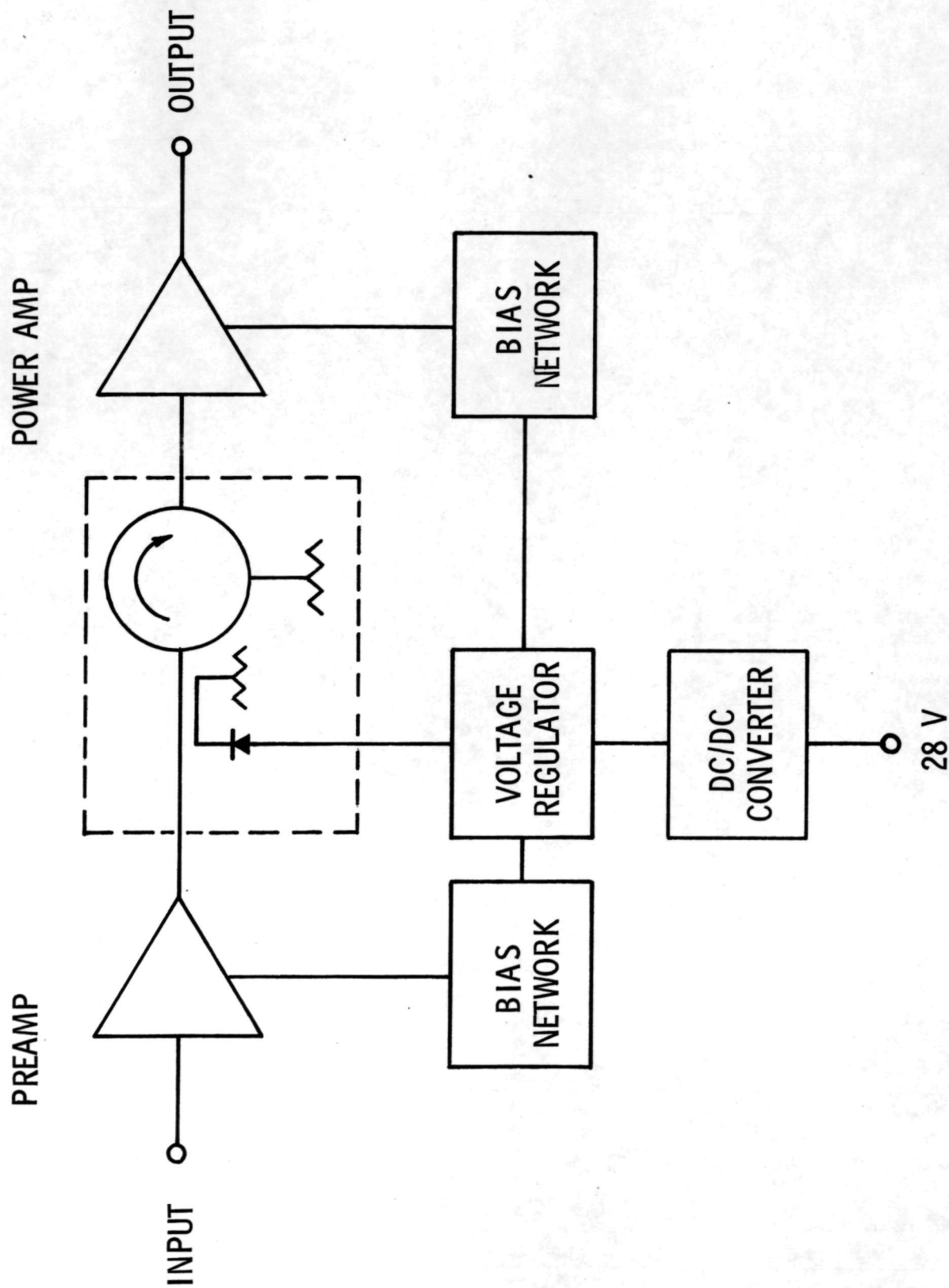


Figure 41 Schematic Diagram of a Stabilization Circuit for Read Amplifier Operation

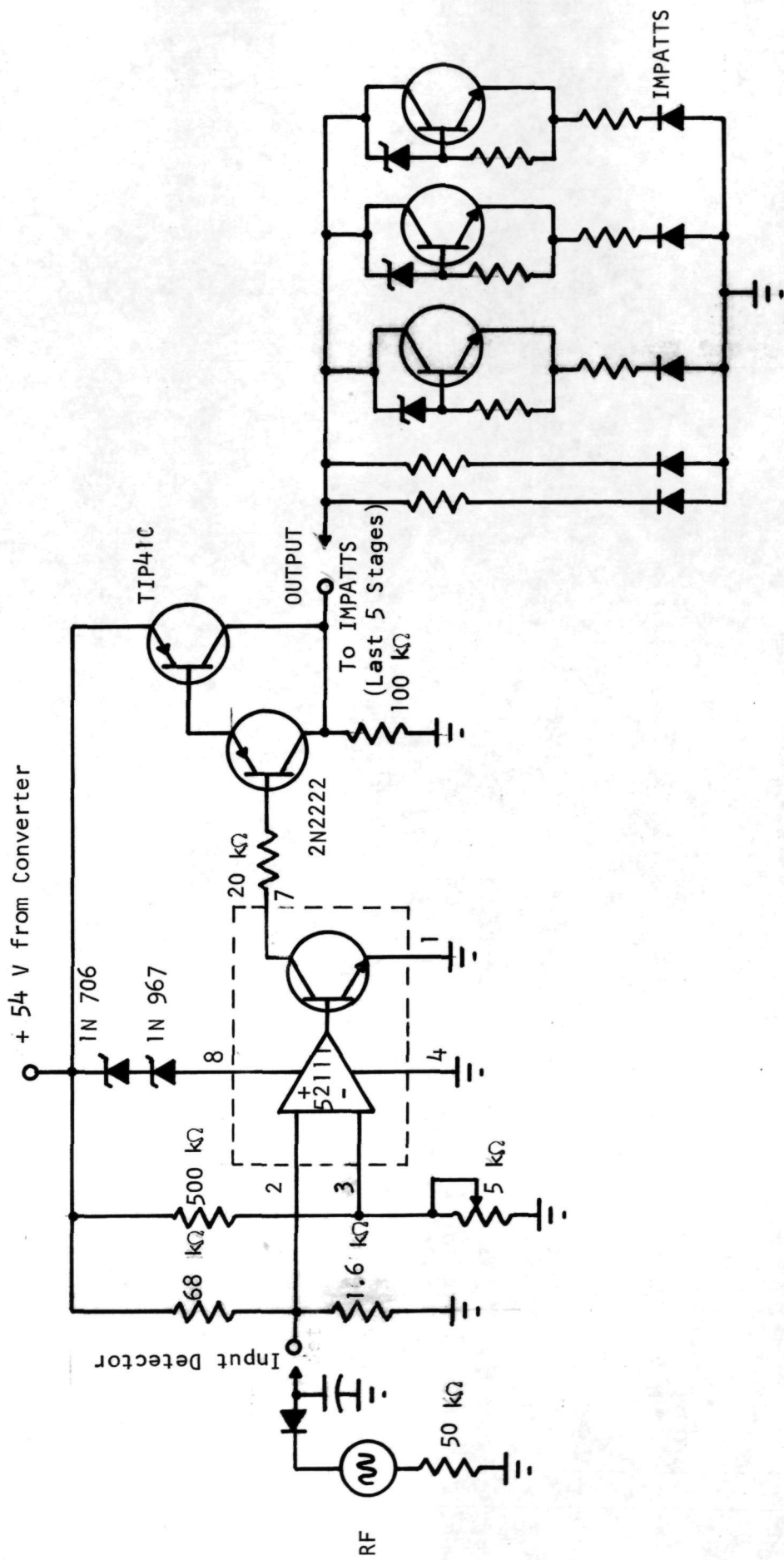
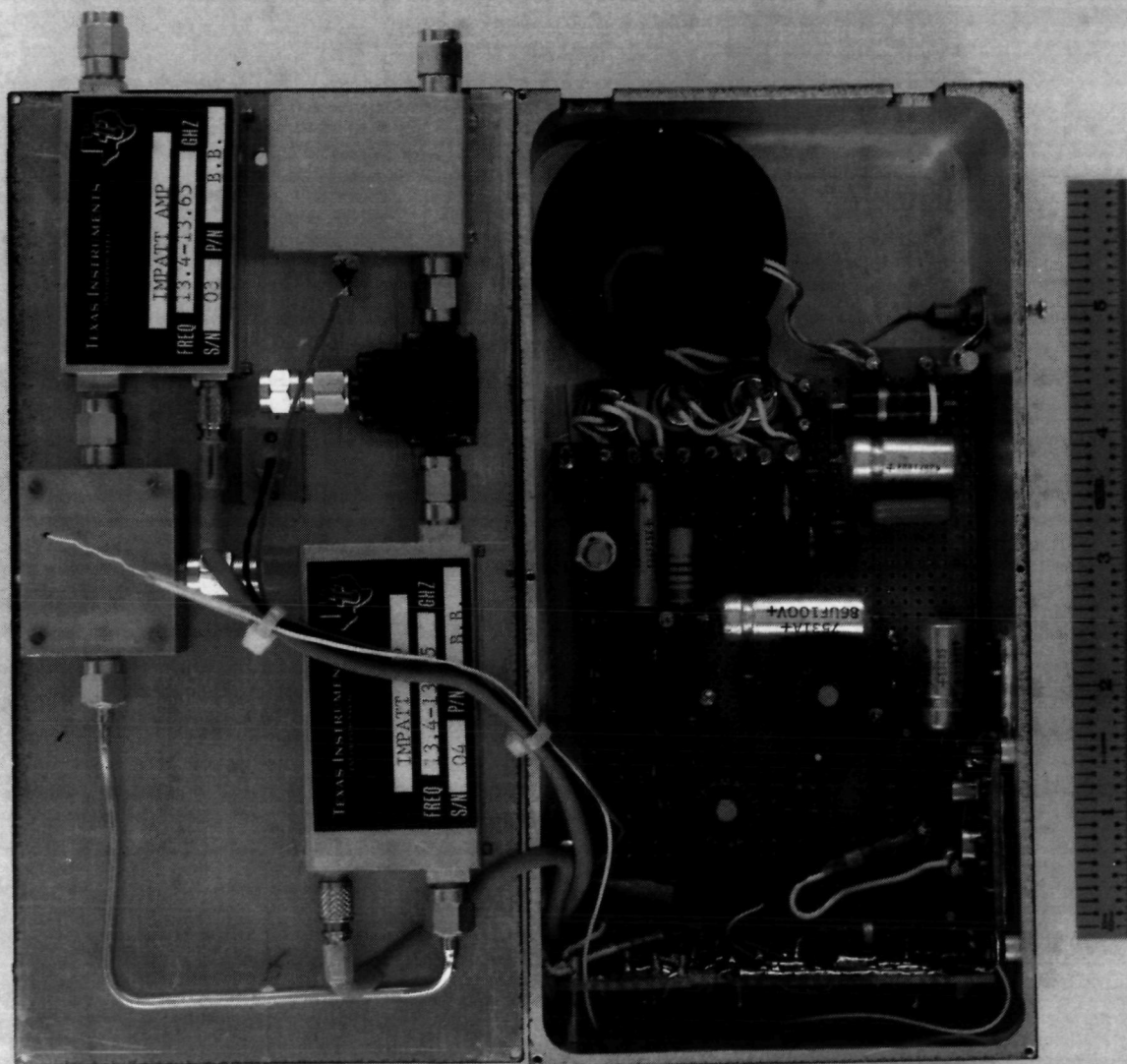


Figure 42 Schematic Diagram of a Power Supply Squelch Circuit

Figure 43 shows a photograph of the Phase II breadboard transmitter module. To improve the stability margin at high output power level, a single-stage output power amplifier was added. An isolator was used between the four-stage power amplifier and the new final output stage. The microstrip isolator-coupler-detector assembly was connected between the preamplifier and the power amplifier. For the Phase II breadboard model, all the amplifier modules and isolators were mounted on a flat plate for easy assembly and testing. The dc/dc converter, voltage regulator, and bias networks were mounted inside the top cover of the transmitter housing. This new module has essentially the same volume as the Phase I module (991 cm^3) described earlier.

Figure 44 shows the gain-frequency response of the Phase II module at three input power levels: -35, -25, and -15 dBm. The power supply squelch circuit has been adjusted to cut off the dc power to the Read stages when the input rf signal drops below a certain level ($\sim -35 \text{ dBm}$) to prevent spurious oscillation. Although the dynamic range of the amplifier will be limited, the stability margin is greatly improved. The module can be powered by an unregulated supply voltage of $28 \pm 1 \text{ V}$. At the highest input drive level of -15 dBm, an output power of 2 W was obtained with 48 dB gain. Due to the unavailability of suitable high-power, high-efficiency Read diodes near the end of the Phase II program, lower power diodes were used for the Phase II breadboard model to meet the delivery schedule. However, it was pointed out in Section II.C that the low-high-low Read diode structure might offer a greater promise for future work. Third-order intermodulation measurements performed on this module indicate a level of -10 to -11 dB at the 2 W output level. Although no extensive measurement of amplifier gain versus temperature was made, it is believed that the thermistor compensation scheme described earlier can partially reduce the temperature sensitivity of the amplifier gain. Although the output power goal of 5 W was not reached for the Phase II model, it is important to note that spurious-free operation was achieved for input power from $\sim -35 \text{ dBm}$ up to a level corresponding to output power saturation. With diode yield improvement, the general circuit techniques can certainly be applied toward achieving the 5 W goal for any future work.



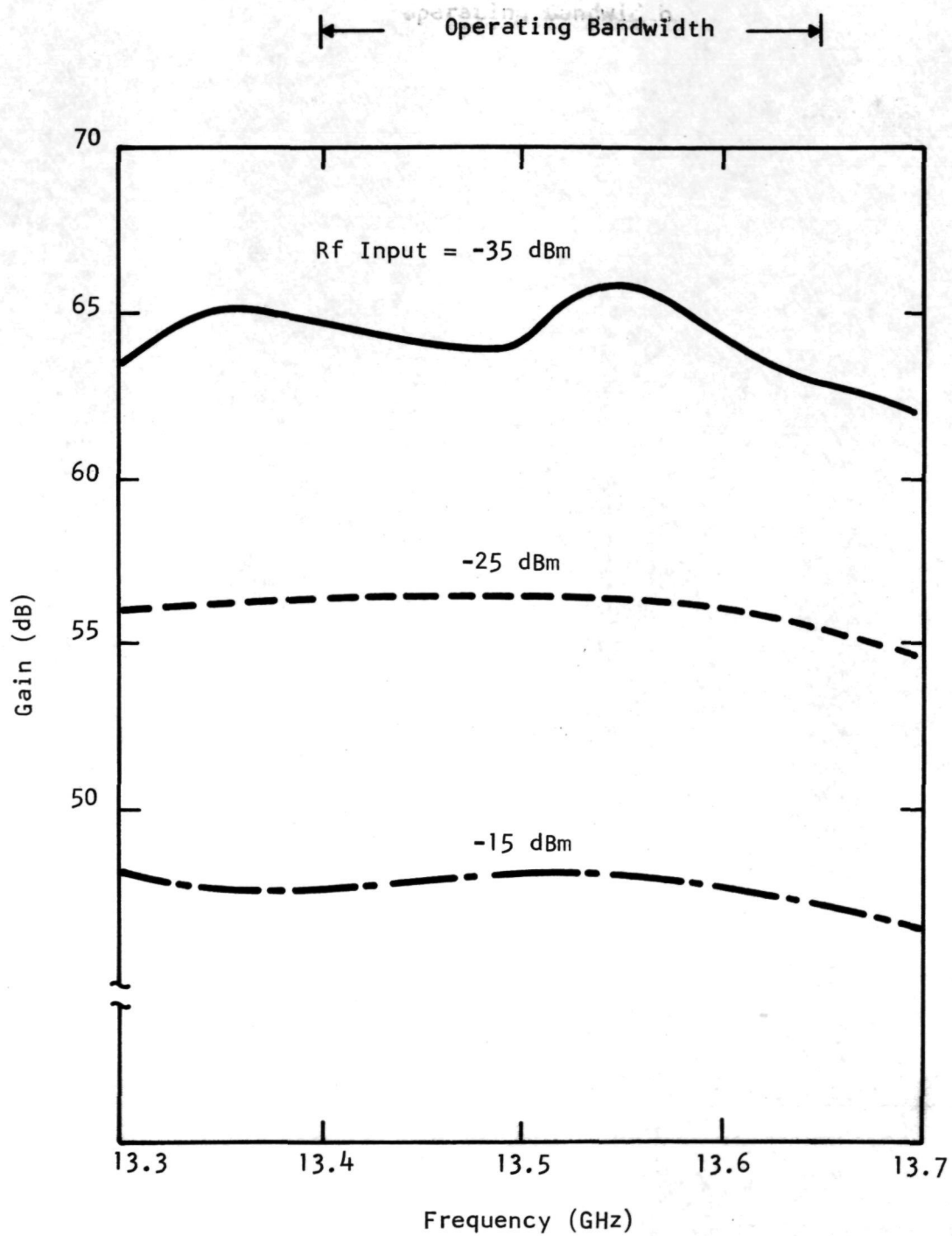


Figure 44 Gain-Frequency Response of Phase II Breadboard Transmitter

SECTION IV

CONCLUSIONS

The goal of Contract No. NAS5-20894 was to develop a Ku-band solid state transmitter. The following conclusions can be drawn with regard to the achievement of the overall objective of the contract.

(1) Wideband (11 to 16 GHz) microstrip circulators can be constructed that are suitable for use in reflection-type amplifiers using GaAs IMPATT and Schottky-Read diodes (first Interim Report).

(2) A compact [$5 \times 3 \times 1.5$ cm ($2 \times 1.2 \times 0.6$ inch)] three-stage IMPATT amplifier can be built in microwave integrated circuit form that will satisfy the preamplifier requirements for the spacecraft transmitter. The major requirements are a gain of 36 dB, a bandwidth of 250 MHz, and a maximum dc input power of 2.5 W.

(3) GaAs Schottky-Read diodes can be operated in a microstrip amplifier circuit in the high-efficiency mode. Single-stage amplifiers utilizing double-mesa Read diodes have produced an output power of 5.9 W with 4 dB gain at 22% efficiency over the frequency band of the transmitter.

(4) A compact [$5.7 \times 3 \times 1.5$ cm ($2.25 \times 1.2 \times 0.6$ inch)], four-stage Read amplifier can be built in microwave integrated circuit form that will satisfy the power amplifier requirements for the spacecraft transmitter. The major requirements are a gain of 21 dB at maximum output power of 5 W, a bandwidth of 250 MHz, and a maximum dc input power of 28 W.

(5) A preamplifier and a power amplifier can be cascaded to achieve an overall gain of 56.5 dB over the frequency band of the transmitter at an output power of 4.5 W. The program goal is 57 dB gain at 5 W output power.

(6) A dc power supply that operates off the available input voltage of 28 ± 1 V can be designed to meet the diode bias requirements and not exceed the maximum available power limit of 50 W. A dc-to-dc converter was built that supplied 54 V with 74% efficiency. Active bias circuits improved the stability of the high power amplifier stages.

(7) A spacecraft transmitter module can be built that meets most of the required specifications. A breadboard transmitter module having 3 W output power with 55 dB gain over the required frequency band was delivered at the end of Phase I. An improved breadboard model incorporating design changes such as the inclusion of a power supply squelch circuit for unconditional stable operation was delivered at the completion of the contract.

In spite of the above success, the yield of Read diodes suitable for the output stages was low. An intensive investigation into the possible reasons for the difficulty in fabricating suitable Ku-band Read diodes for microstrip amplifier application has led to the following conclusion regarding future diode work for spacecraft transmitter applications.

GaAs Read diodes designed with a high-low doping profile to operate at Ku-band frequencies have not shown the high performance that has been obtained at X-band frequencies. It is apparent that a lightly doped drift layer results in efficient devices, but that these devices are difficult, if not impossible, to utilize in common circuits at Ku-band frequencies. It has been shown that a higher doping in the drift layer results in higher frequency devices. Furthermore, a drift doping profile that is flat, with no gradient toward the substrate, has been shown to be even more important at Ku-band than at X-band. This necessitates a rapid transition in doping profile from the buffer layer into the drift.

With increased drift layer doping, it would be desirable to increase the high layer doping also, to maintain the large high-low ratio necessary for high efficiency performance. However, the high-layer doping cannot be increased without bound, since this enhances tunnel injection at the Schottky barrier contact. The tunnel current retards the phase of the injected charge in the device to a degree that competes with the potentially increased efficiency that may be obtained by increasing the high-low ratio.

Since the increased drift doping is required to maintain the high frequency response, it is necessary to resort to a device structure that shortens the length of the avalanche region while simultaneously reducing the magnitude of the field strength at the Schottky barrier contact. This can be accomplished by using a low-high-low structure. Previous work at X-band frequencies showed approximately equal results from both high-low and low-high-low structures. The experience gained in the previous work can be readily adapted to the growth of low-high-low structures suitable for Ku-band devices. Several characterization wafers have already been grown with the low-high-low profile so that a full comparison of the two device types may soon be made at Ku-band.

REFERENCES

1. W. T. Read, Jr., "A Proposed High-Frequency Negative-Resistance Diode," Bell Syst. Tech. J. 37, 401 (1958).
2. W. R. Wisseman, D. W. Shaw, R. L. Adams, and T. E. Hasty, "GaAs Schottky-Read Diodes for X-Band Operation," IEEE Trans. Electron Devices ED-21, 317 (1974).
3. W. C. Niehaus and B. Schwartz, "A Self-Limiting Anodic Etch to Voltage (AETV) Technique for Fabrication of Modified Read IMPATTs," J. Electrochem. Soc. 121, 207C (1974).
4. N. J. Tolar, "Fabrication of Semiconductor Devices Having Low Thermal Impedance Bonds to Heat Sinks," U. S. Patent 3,689,993, issued September 12, 1972.
5. B. C. DeLoach, "A New Microwave Measurement Technique to Characterize Diodes and an 800-Gc Cutoff Frequency Varactor at Zero Volts Bias," IEEE Trans. Microwave Theory Tech. MTT-12, 15 (1964).
6. C. E. Fay and R. L. Comstock, "Operation of the Ferrite Junction Circulator," IEEE Trans. Microwave Theory Tech. MTT-13, 15 (1965).
7. H. Q. Tserng, D. N. McQuiddy, and W. R. Wisseman, "X-Band MIC GaAs IMPATT Amplifier Module," IEEE J. Solid-State Circuits SC-10, 32 (1975).
8. H. Q. Tserng and D. N. McQuiddy, "Ku-Band MIC GaAs IMPATT Amplifier Modules," 1976 International Solid-State Circuits Conference, Digest of Technical Papers, pp. 78-79, February 1976.